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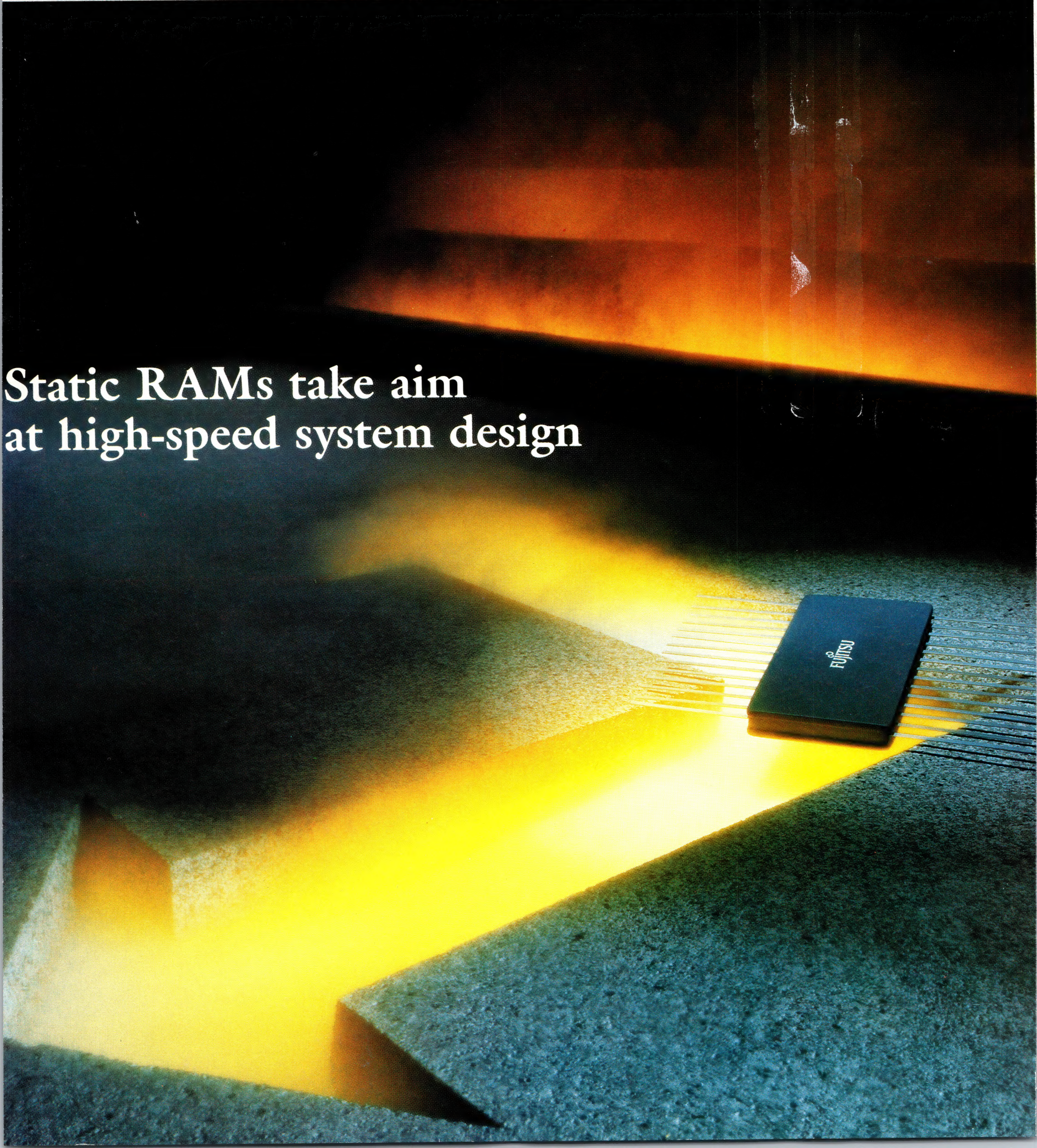
Designer's guide to op-amp macromodels

IR thermometers for noncontact measurement

Engineering in the UK

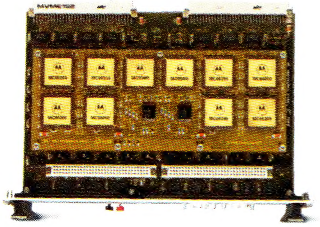
Fiber-optic connectors satisfy exacting needs

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Static RAMs take aim at high-speed system design

and a full 32-bit VMEbus interface. Performance rated at up to 21 MIPS.



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enclosure. Performance rated at 17 MIPS.

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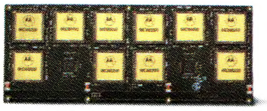

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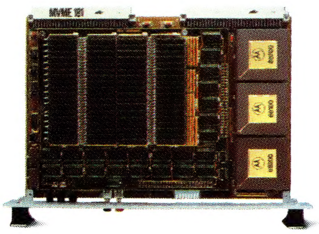

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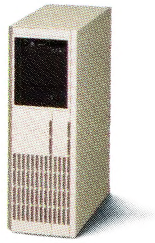

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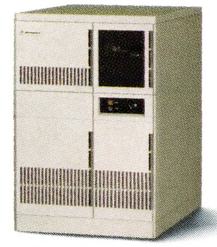

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EDN® Magazine Edition

Volume 35, Number 4

February 15, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *When you choose a static RAM for your high-speed system, consider how different memory devices will affect your design. See the Special Report on pg 126. (Photo courtesy Fujitsu Microelectronics; concept and photography by Imagination)*

SPECIAL REPORT

Static RAMs 126

As processing speeds exceed 30 MHz, the memory devices in your system pose design problems of their own. At these speeds, traces act like transmission lines, so reflections, ground bounce, crosstalk, and signal degradation all become critical factors in your design.—*J D Mosley, Regional Editor*

Modern spirit, traditional reserve: The character of a British electronics company 65

This article, the second in an occasional series that examines the electronics-engineering profession in Europe, looks at Marconi Instruments in England. —*Gary Legg, Special Projects Editor*

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DESIGN FEATURES

Designer's guide to Spice-compatible op-amp macromodels—Part 1 143

Part 1 of this 2-part article shows how the existing macromodels of op amps are inadequate for simulation of today's fast devices and describes a new approach that yields improved ac- and transient-simulation accuracy.—*Mark Alexander and Derek F Bowers, Precision Monolithics Inc*

Use a counter to characterize rapidly changing signals 159

You can greatly simplify characterizing dynamic and transient signals by using a universal counter that combines high precision and a fast measurement rate.—*Lewis W Masters, Guide Technology Inc*

Nonlinear components lower settling time of noise-reduction filters 177

Noise filtering often causes an increase in settling time, but the proper application of a nonlinear filter can speed data acquisition by 4 to 1 over simple RC filters.—*Rod Burt and R Mark Stitt, Burr-Brown Corp*

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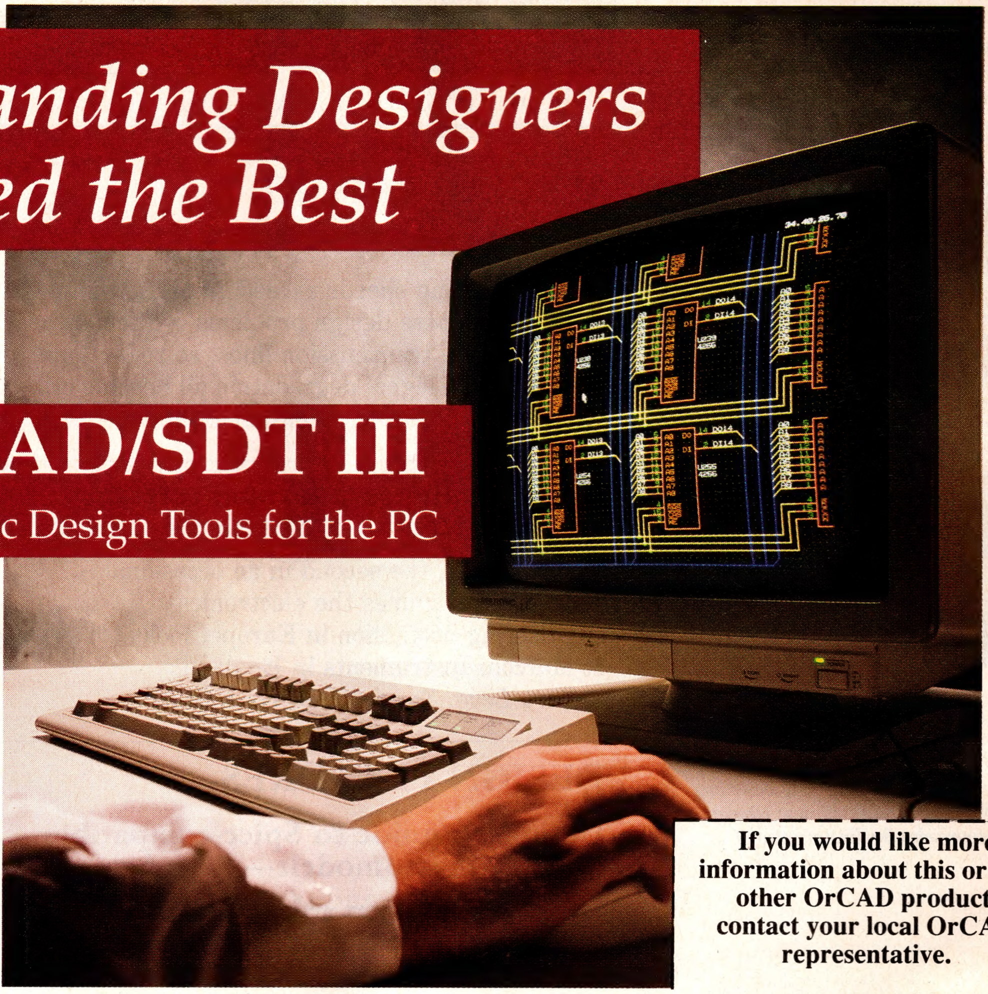

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IR-radiation thermometers let you monitor the temperature of targets with refined accuracy and without damaging fragile bodies.—*John A Gallant, Associate Editor*

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Many available graphics libraries simplify the task of meeting end users' graphics requirements and allow you to reuse your designs in similar development systems.—*Chris Terry, Associate Editor*

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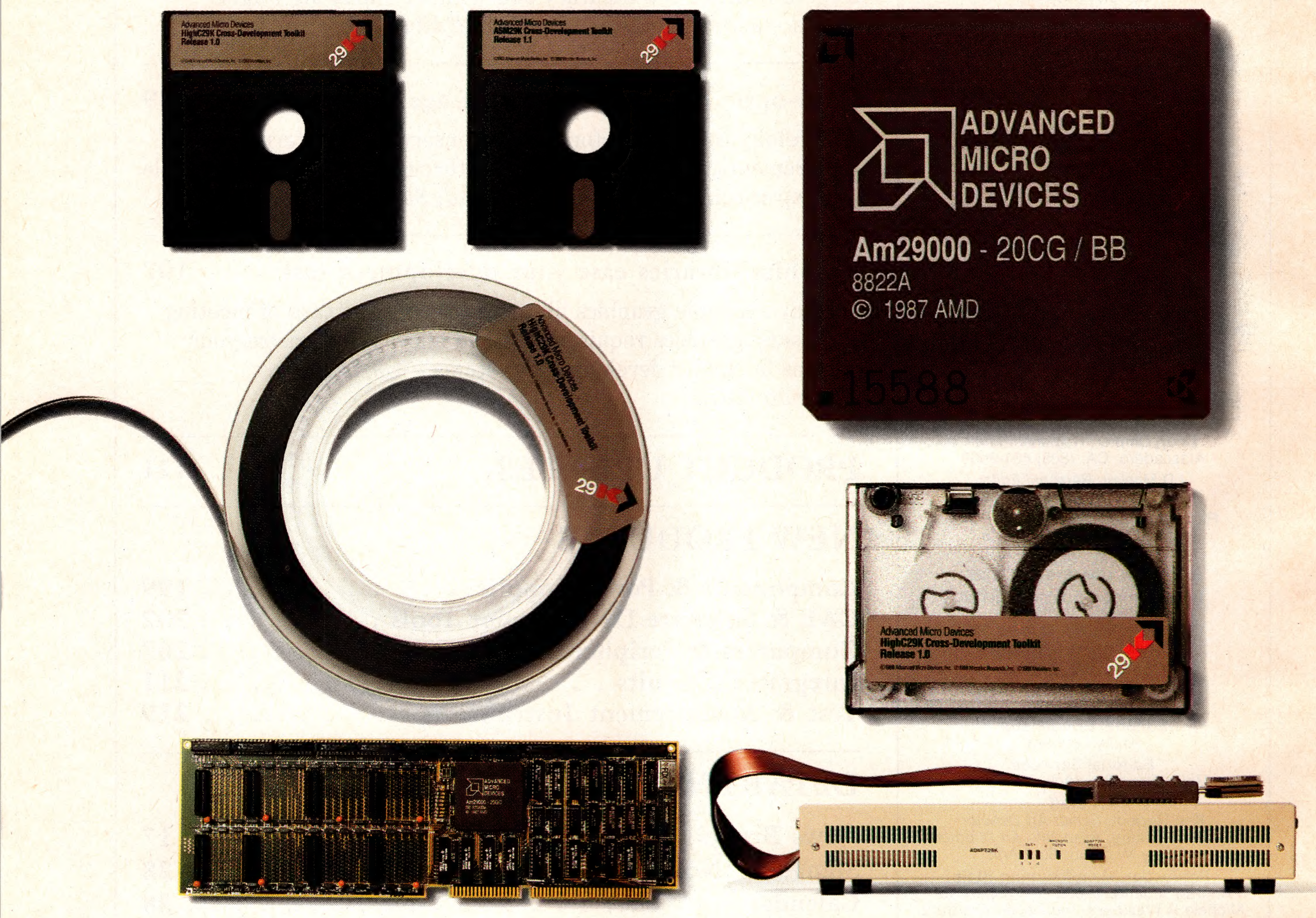

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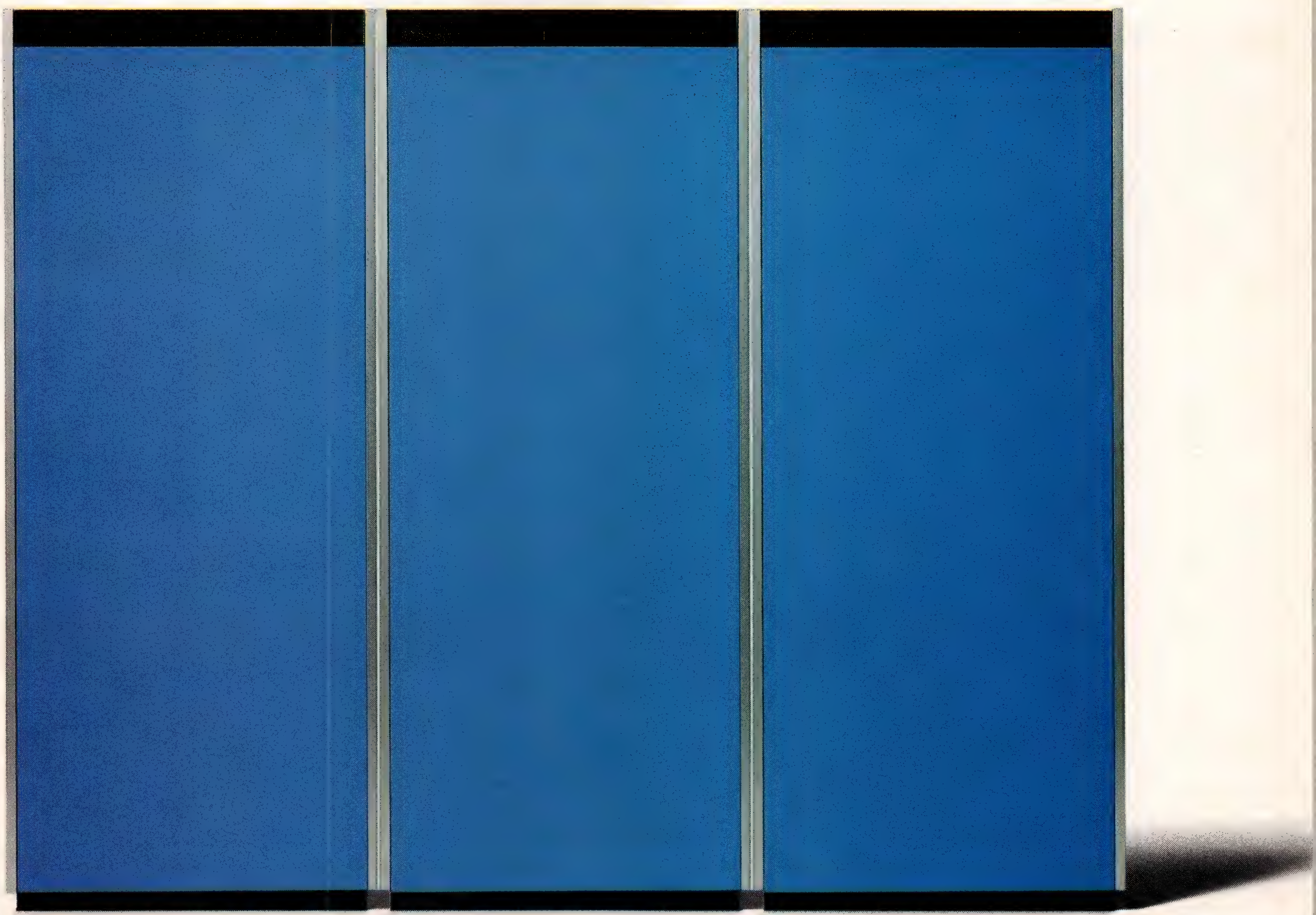

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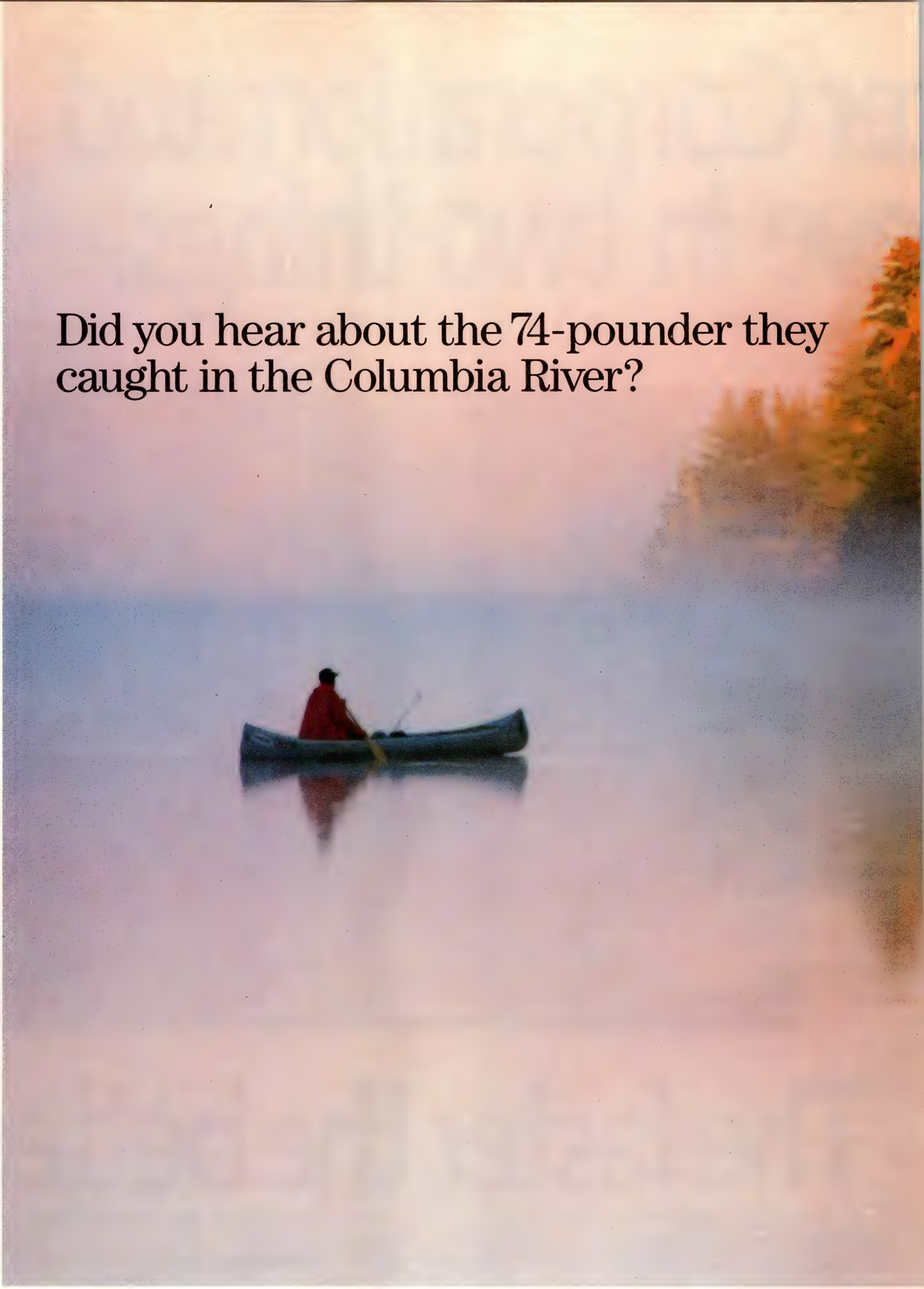
Did you hear about the 74-pounder they caught in the Columbia River?

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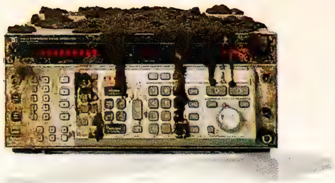

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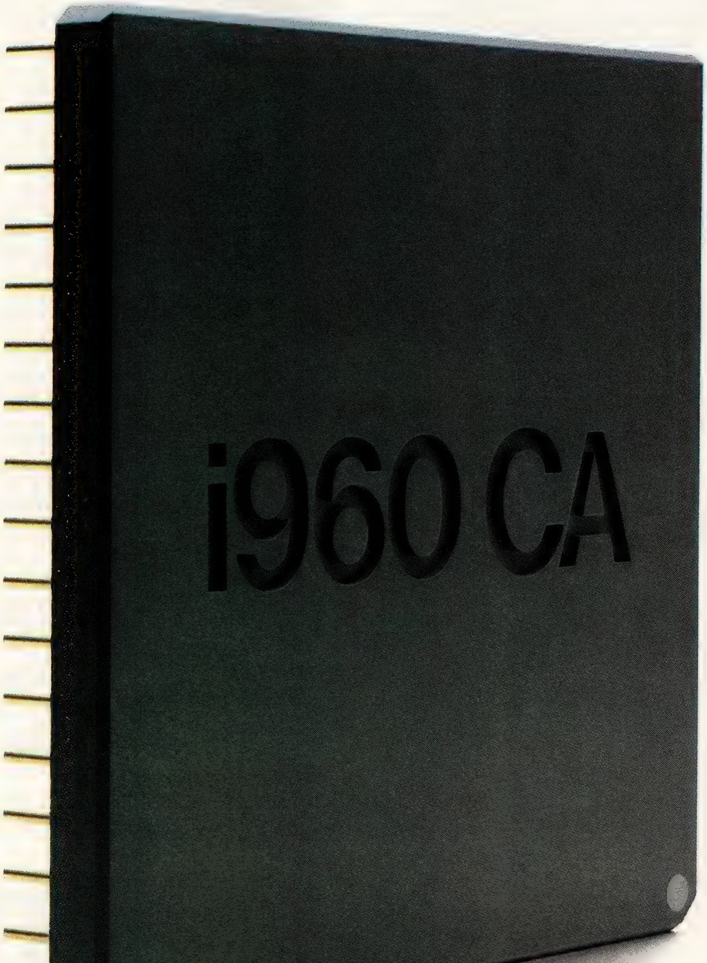

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It's a milestone.

Multiple instructions per clock is now a reality. Intel's new i960 CA is the first 32-bit embedded processor to execute multiple integer and control instructions per clock.

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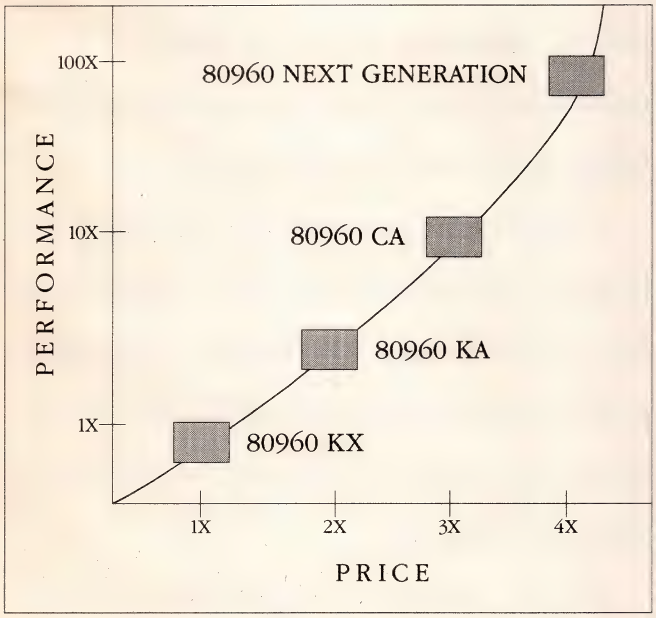

For 32-bit embedded control, i960 architecture offers a broad and growing range of price-performance options.

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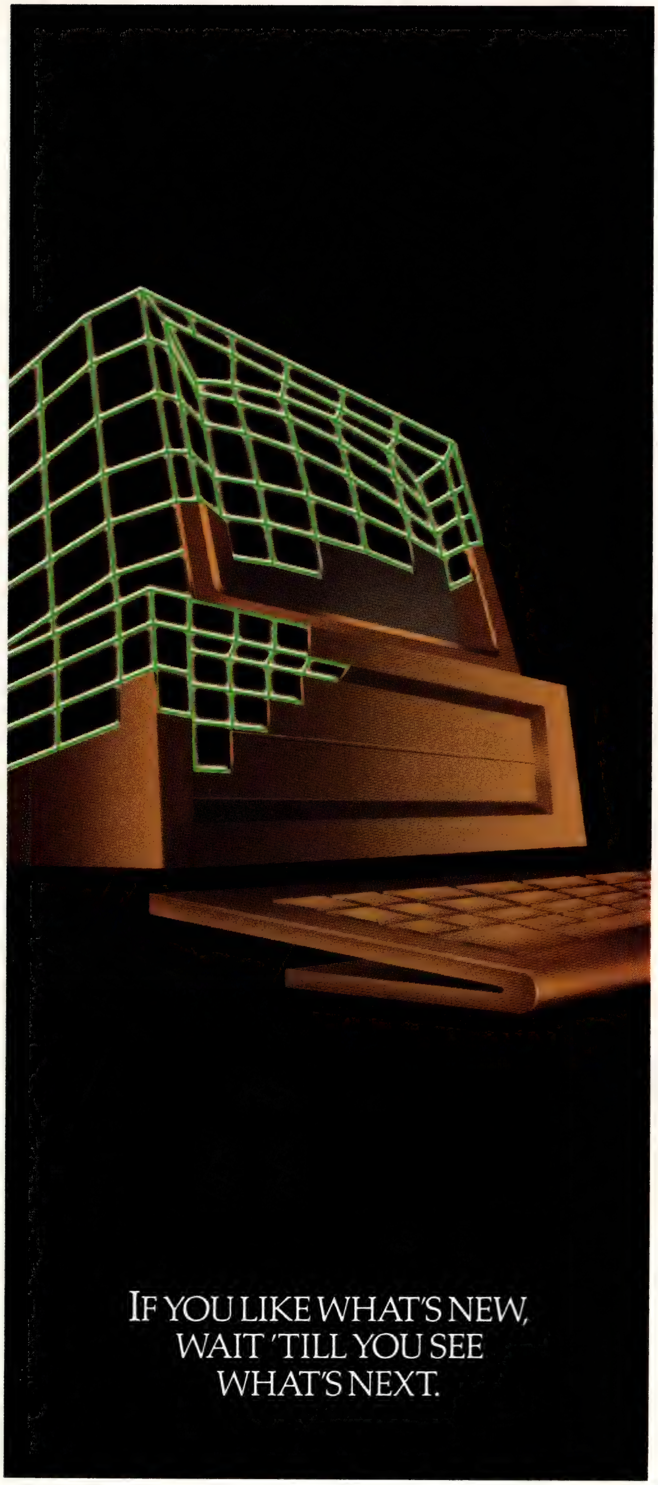

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4K x 4	MCM4180	18, 20, 25ns	PDIP, PSOJ
4K x 4	MCM62350	18, 20, 25ns	PDIP, PSOJ
4K x 4	MCM62351	18, 20, 25ns	PDIP
Synchronous Fast Static RAMs			
64K x 4	MCM62980/2*	20, 15ns	PSOJ
4 x 64K x 1	MCM62981/3*	20, 15ns	PSOJ
16K x 16	MCM62990†	20, 25ns	PLCC
16K x 4	MCM6293/4/5	20, 25, 30ns	PDIP, PSOJ
4K x 12	MCM62973/4/5	20, 25, 30ns	PLCC
DSPRAM™			
8K x 24	MCM56824†	25, 35ns	PLCC
Latched Fast Static RAMs			
8K x 20	MCM62820†	23, 30ns	PLCC
16K x 16	MCM62995†	20, 25ns	PLCC
Fast Static RAM Modules			
64K x 32	MCM3264†	20, 25ns	64 ZIP
256K x 8	MCM8256†	20, 25ns	60 ZIP
2 x 64K x 24	MCM2464†	20, 25ns	58 ZIP

☆Samples now introduction in 1Q90
† Samples in 1Q90 introduction in 2Q90
*Samples in 2Q90 introduction in 3Q90

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NEWS BREAKS

EDITED BY JULIE ANNE SCHOLFIELD

SPEED UP, POWER DOWN IN MICROCHANNEL INTERFACE EPLD

Altera Corp (San Jose, CA, (408) 984-2800) has increased the speed and reduced the power requirements of its Micro Channel Architecture (MCA) interface IC, the EPB2001. This EPLD (electrically programmable logic device) performs address decoding in 25 nsec—the earlier version needed 35 nsec—and responds to control strobes in 18 nsec instead of 25 nsec. The device's supply current dropped from 100 to 30 mA. The device handles the interface functions for an IBM PS/2 add-in card and provides programmable address decoding and board identification. It costs $43.25 (1000) in a windowed ceramic package; the one-time-programmable version costs $17 (1000).—Richard A Quinnell

STE BUS CPU SPEEDS TO 4 MIPS AND UPGRADES TO VMEbus

Claiming that 8-bit bus structures satisfy most industrial-control needs, STEbus proponent Arcom Control Systems (Cambridge, UK, FAX 223-410457) announced a 68020-based CPU module promising 4 MIPS. The SC020T (£745) crams a 32-bit, 16-MHz subsystem onto a single Eurocard. The memory comprises 512k bytes of 32-bit wide static-RAM (SRAM) and 32k bytes of battery-backed SRAM. The board can also accommodate 512k bytes of 16-bit-wide EPROM. The board includes a watchdog timer, real-time clock, arbitration logic for master/slave operation, and dual RS-232C ports.

If choosing an 8-bit system would box you in, the VSC020T (£1095) is also on hand. This combined STE Bus and VMEbus double-Eurocard CPU module boasts SC020T compatibility. As design requirements change, you can swap CPU hardware to match your system needs. Thus, you have a neat upgrade path without dumping existing STE Bus I/O and signal-conditioning hardware.—Brian Kerridge

SPACE STATION FREEDOM WILL FLY REAL-TIME UNIX OS

Computers on the Space Station Freedom will use a real-time Unix-compatible operating system called LynxOS from Lynx Real-Time Systems Inc (Campbell, CA, (408) 370-2233). IBM, the subcontractor developing Space Station Freedom's data-management system for McDonnell Douglas Space Systems Co, selected LynxOS after testing three competing operating systems for more than a year. IBM based its selection on criteria such as operating speed, code size, and conformity to a variety of standards including POSIX (the portable operating-system interface for computer environments, IEEE 1003.1), real-time extensions to POSIX (IEEE 1003.4), and Ada bindings for POSIX (IEEE 1003.5). Space-station development projects employ Ada as the programming language of choice by NASA fiat. Lynx offers LynxOS for several µPs including Motorola's 68030 and 88000 and Intel Corp's 80386.—Steven H Leibson

PIN DRIVERS AND ACTIVE LOAD HANDLE HIGH-SPEED SIGNALS

Two pin drivers and an active-load device from Analog Devices (Norwood, MA, (617) 329-4700) can test ECL, TTL, and CMOS logic at high signal speeds. The AD1321 ($89) and AD1322 ($169) pin drivers, respectively, feature 100- and 200-MHz operation, 1V/nsec and 2V/nsec slew rates, and 200- and 250-psec edge matching. The drivers have unity-gain programmable output levels of −2 to +7V with an output swing of 100 mV to 9V. The AD1315 ($80) active-load device has a ±50-mA voltage-programmable current range and a 1.5-nsec propagation delay. All three devices feature an inhibit mode that limits the leakage current of the pin drivers to 50 nA typ and the active-load device to 20 nA typ. Each device comes in a 16-lead, hermetically sealed gull-wing package and operates from 0 to 70°C.—Anne Watson Swager

EDA SYSTEM UNITES CAD/CAM AND CAE/CAT TOOLS

Racal-Redac (Tewkesbury, UK, FAX 734-668206) threatens the lead position of Mentor Graphics and Dazix in electronic-design automation (EDA) with its Visula Plus CAE system. The software suite blends the Visula Plus pc-board CAD/CAM core with the CADAT digital simulator and Saber analog simulation. The system's net lister and hypermodels allow concurrent operation of CADAT and Saber for mixed-mode simulation. Users access the data library by a generic component title, a company part number, or whatever the library manager has set up. Simulation is possible concurrent with schematic capture, and you can view the results simultaneously. Worst-case timing analysis lets you adjust individual propagation spreads and view cumulative effects. With a Sun SPARCstation as the recommended workstation, a LAN accelerator links adjacent workstations and the CATS hardware modeler. Prices start at £25,000.—Brian Kerridge

ECL PROCESS INTEGRATES 150,000 GATES ON ONE CHIP

Bipolar Integrated Technology Inc's (Beaverton, OR, (503) 629-5490) next-generation bipolar technology can put 150,000 ECL gates on a single chip. Chips produced by the P201 process operate at 40 µA/gate with gate delays shorter than 200 psec per loaded gate. This triple-implanted self-aligned process features a 10-GHz transistor and uses 13 masks for a 3-layer metal design, including the final passivation. Self-isolation and self-alignment result in what the company claims are the smallest bipolar transistors available. The metal pitch for the first two layers is 2.4 µm, which results in shorter metal runs and lower interconnect loading than other bipolor technologies. Designers can take advantage of this technology via the company's standard-cell library.—Julie Anne Schofield

ISOLATED DC/DC CONVERTER MODULES COST $17

Two families of converter modules from Burr-Brown Corp (Tucson, AZ, (602) 746-1111, FAX (602) 889-1510) provide isolated dc/dc conversion for as little as $17 (100). The PWR40XX series comprises 12 devices that have 5, 12, 15, and 24V dc inputs. Single-output models in this series generate 5V dc; dual-output models generate ±12 or ±15V. All models in this series are rated at 4W. The two devices in the company's PWS72X series transform 5 or 15V into ±15V. Converters in the PWR40XX series provide 500V dc isolation between inputs and outputs and are available in a high-voltage version rated at 1000V dc isolation. Converters in the PWS72X series provide 750V rms isolation and are 100% tested to withstand 1200V rms.—Steven H Leibson

WORKSTATIONS OFFER CHOICE OF GRAPHICS PROCESSOR

Although many workstation vendors are selecting Motif and Open Look as their graphical user interfaces, Intergraph Corp (Huntsville, AL, (205) 730-8301) selected Looking Glass. The company's 6000 Series workstations feature a choice of graphics processor. One of these graphics processors offers eight planes of double-buffered

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graphics plus a highlight plane and as many as 256 colors from a palette of 16.7 million colors. This lower-end processor draws 110,000 2-D vectors/sec and supports Gouraud shading at 1000 100-pixel triangles/sec. The other graphics processor provides 24-bit color and offers 16.7 million colors from a 16.7-million color palette. This high-end processor supports drawing rates of 400,000 2-D vectors/sec and Gouraud shading at 25,000 100-pixel triangles/sec. A 10-MIPS 6040 workstation with lower-end graphics, 16M bytes of RAM, and a 355M-byte hard disk costs $29,900. A 14-MIPS InterPro 6280 with high-end graphics, 16M bytes of RAM, and a 670M-byte hard disk costs $45,900.—Michael C Markowitz

125-MHz FIELD-PROGRAMABLE GATE ARRAYS AVAILABLE

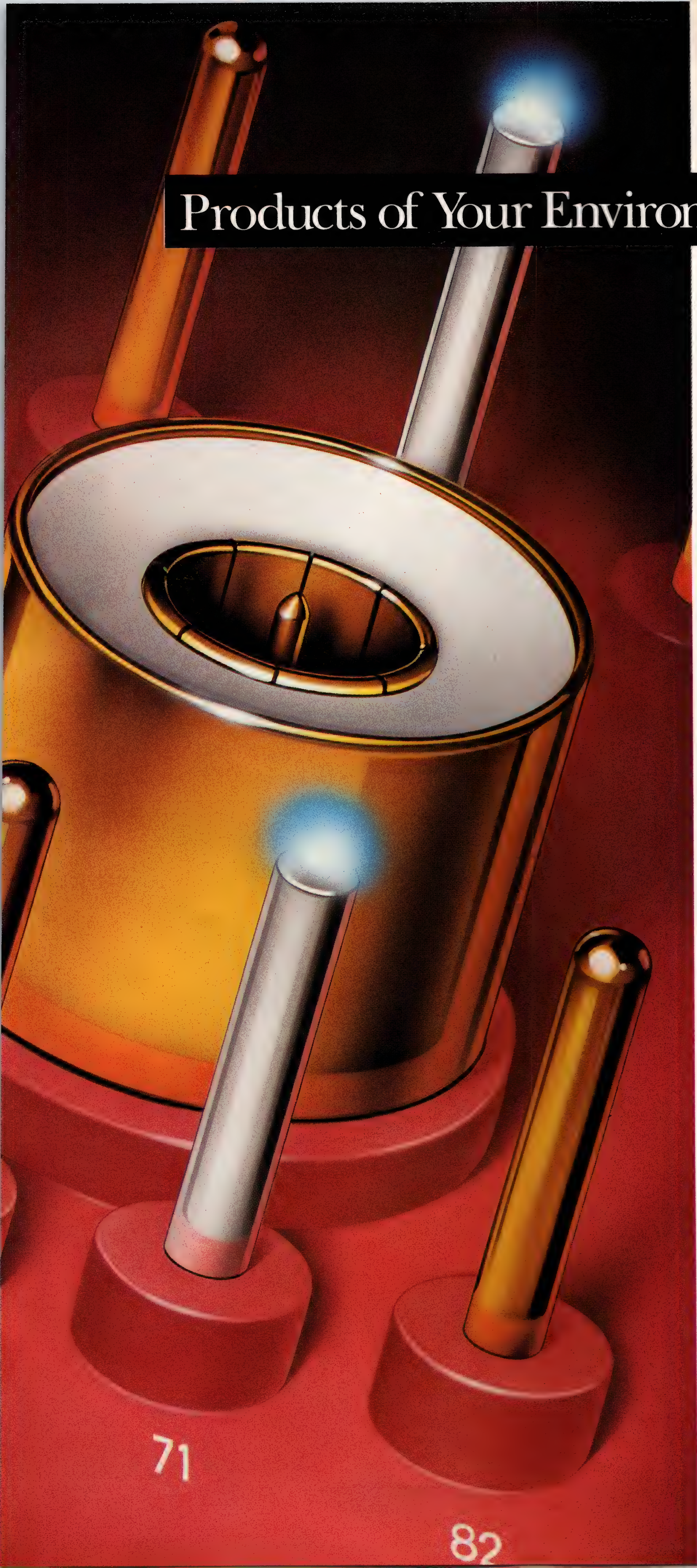
Advanced Micro Devices Inc (Sunnyvale, CA, (800) 222-9323) is offering samples of the industry's fastest field-programmable gate arrays (FPGAs). The devices feature "toggle rates" of 125 MHz, but attainable system speeds tend to be about 20 to 30% or less of the FPGA toggle rate. The devices use standard static-RAM cells as programming elements. These faster FPGAs can increase the percentage of the chip used because longer routing paths can be employed without crippling the chip's performance. Samples of the 125-MHz, 2000-gate-equivalent Am3020-125 are available now in an 84-pin plastic leaded chip carrier. Production volumes will be available in May for $50.36 (100). The company will start upgrading other FPGAs to 125 MHz in the second quarter of this year. These parts, featuring as many as 9000 gates, will be in volume production in the third quarter.—Julie Anne Schofield

EUROPEAN COMPANY DEBUTS CMOS 64k-BIT SRAMs

A range of CMOS SRAMs (static RAMs) from Philips Components (Eindhoven, The Netherlands, 40 724324) offers low power consumption and fast access times. You can select from two 8k-byte × 8-bit devices that have 70-nsec access times. The standby current for the standard FCB61C65-70P and the low-power FCB61C65L-70P is 3 mA and 100 μA, respectively. The parts come in 28-pin DIPs having standard pinouts. The parts cost gld 10 (100). The company is targeting an ultralow-power version with a standby requirement of 1 μA at 3V for the second quarter of this year. Initially, the part will be available in an SO28XL package. Standard-power SRAMs with access times of 55 nsec will follow midyear.—Brian Kerridge

HARDWARE VENDOR UNIFIES DESIGN-MANAGEMENT FRAMEWORK

Strengthening what had already been an OEM relationship, Digital Equipment Corp (Maynard, MA, (508) 467-5164) announced the acquisition of EDA Systems' (Santa Clara, CA, (408) 986-9585) PowerFrame and customer-support and OEM contracts. Digital also announced its DECframe/Electronics version of PowerFrame, a design-management framework. Unlike a design-data framework, a design-management framework ensures revision control, adherence to a design methodology, and protection of project data in an environment that is transparent to the user. DEC's software package adds such features as multistation workgroup support, design-release management, and design checkpointing to PowerFrame. The software supports three third-party packages: the ValidGED graphics editor, Allegro pc-board software, and the Verilog simulator. Pricing starts at $5525 for software that runs on a stand-alone DECstation; versions for Sun, Apollo, and Hewlett-Packard workstations will soon be available.—Michael C Markowitz



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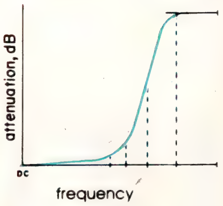
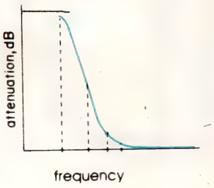


MODEL NO.	PASSBAND, MHz (loss <1dB)	fco, MHz (loss 3db)	STOP BAND, MHz (loss>20dB)	STOP BAND, MHz (loss>40dB)		VSWR		PRICE $ Qty. (1-9)
	Min.	Nom.	Max.	Max.	Min.	pass-band typ.	stop-band typ.	
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz

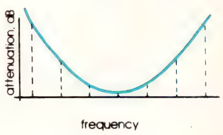
HIGH PASS



MODEL NO.	PASSBAND, MHz (loss <1dB)		fco, MHz (loss 3db)	STOP BAND, MHz (loss>20dB)	STOP BAND, MHz (loss>40dB)	VSWR		PRICE $ Qty. (1-9)
	Min.	Min.	Nom.	Min.	Min.	pass-band typ.	stop-band typ.	
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz

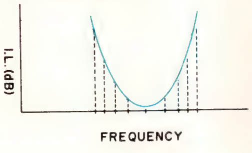
BANDPASS



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB)		STOP BAND, MHz (loss > 10 dB)		STOP BAND, MHz (loss > 20 dB)		VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
		Max. F1	Min. F2	Min. F3	Max. F4	Min. F5	Max. F6		
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF

NARROWBAND IF



MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB		STOP BAND, MHz I.L. > 35dB		PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
			F5	F6	F7	F8-F9		
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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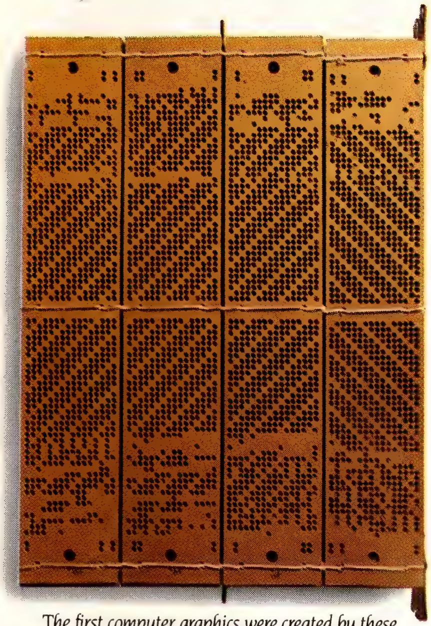

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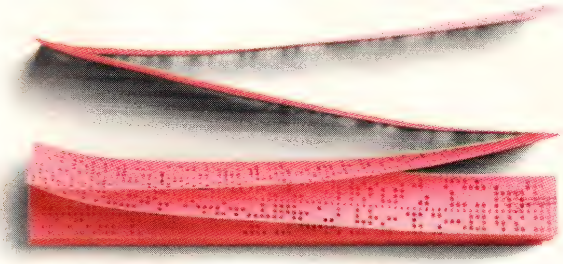

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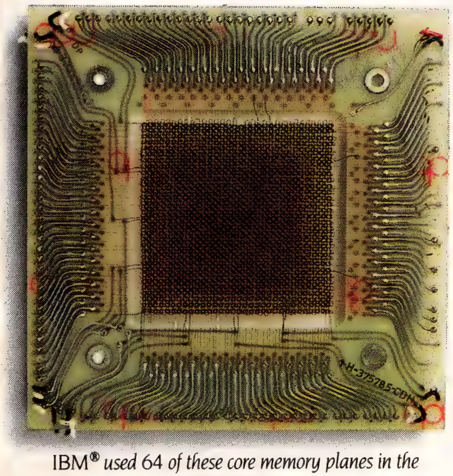

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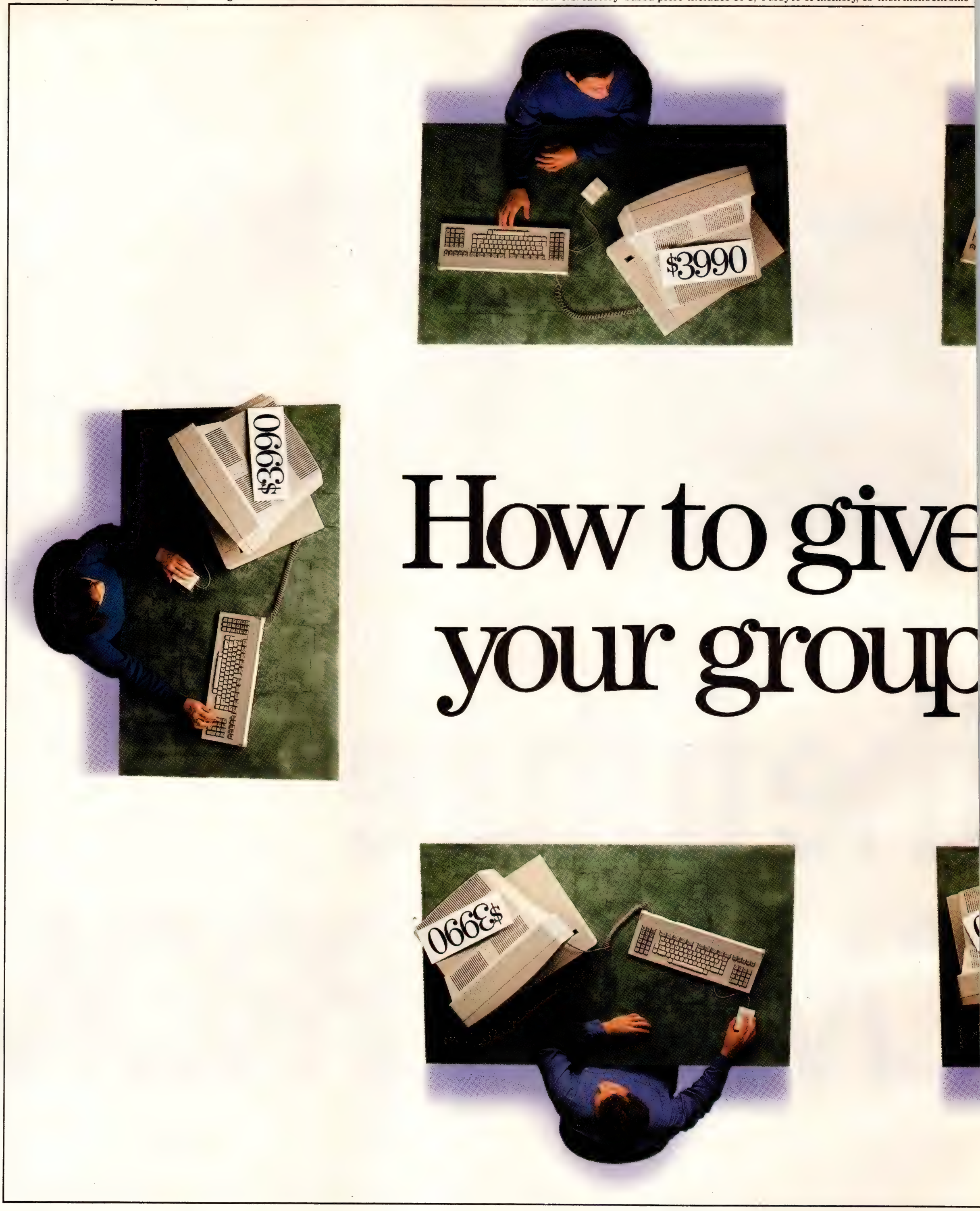
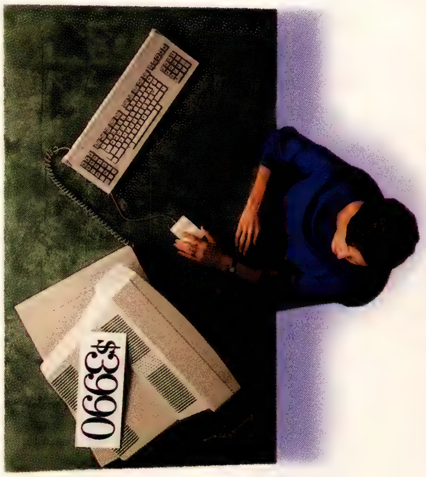
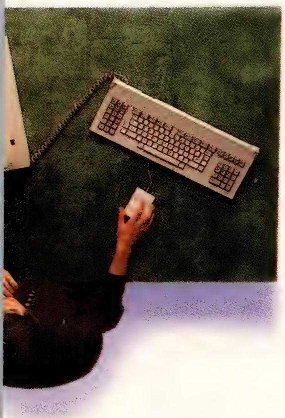


nonitor, and a choice of network controllers (Ethernet, IBM token ring or Apollo Token Ring) but excludes shipping. ©1990 Hewlett-Packard Company CPWG921

everyone in
a workstation.





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SIGNALS & NOISE

Another view on sending alien graduates home

In his letter in EDN (August 17, 1989, pg 33), I believe reader M Kamal Khan is missing the point of an excellent editorial by Jon Titus on sending alien graduates home (EDN, October 27, 1988, pg 57). The issue is not "naturalized citizenship" at all. Jon's message was clear: a student of foreign nationality who enters the United States with the stated intention of obtaining a US technical education is receiving a privilege. This opportunity, to a large extent, is funded by US taxpayers whose children, thanks to foreign competition for enrollment, may then not be able to enjoy the advantages of the college education they have partially paid for.

For the privilege of studying in the United States, alien students are required to sign an agreement that they will return to the country of their origin. The intent of this pact is neither to punish the alien student nor is it necessarily aimed at protecting the US economy. The goal is simply to bring to the country of the student's origin new technology so that more than one person may benefit from the fruits of US research and development dollars.

This fact is often overlooked by our temporary foreign-guest students. There is an old adage, "Give a man a fish, and he has food for a day. Teach that man to fish, and his family can eat for life." If a student is sponsored to learn a sorely needed trade, and then that student absconds with the knowledge, the act is semitreasonous, or at the very best, shows a mercenary lack of fidelity to one's roots.

Foreign students who complain about conditions in their native land, leave their country under the guise of gaining an eduction, and then do not return to try to improve conditions there, remind me more of rats deserting a sinking ship than "technologists," "scientists," or "doctors."

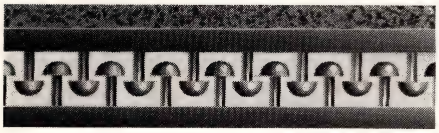
N Silber
Cedar Grove, NJ

Plotter gives edge to small company

The Product Update, "Prototyping systems produces pc boards in one day" (EDN, November 9, 1989, pg 116) on the use of a plotter for the application of pc-board resistance, was interesting to us.

For the past four or five years, we have been using a Leading Edge 8088 computer, Wintek Smartwork software, and a Western Graphtec

Faster fasteners for access panels.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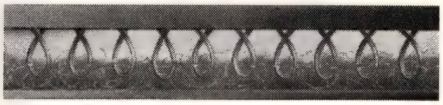
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Beveled Glass Window by
Thomas Tisch & Andreas Lehmann
Oakland, California

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2000 tabletop plotter. We use Smartwork for our pc-board design, and when finished, "flip" the image. We then place a .032 copper-clad G-10 (to 12×12 in.) on the plotter table (in place of paper); instruct Smartwork to plot a 1:1 image; install a pen holding waterproof ink; and in 30 minutes have a prototype design ready to etch in our tabletop etcher.

We can often go from a concept of a simple design to an etched, drilled, assembled prototype pc board in 4 hours. For small engineering/design companies like us, this capability gives us amazing flexibility and an edge over larger inflexible competition. (We need all we can get.)

Steve Moe
Intercity Electronics Inc
Eugene, OR

Correction

On pg 58 of the article entitled "182 VXIbus products appear from 36 firms" (EDN, November 23, 1989, pg 51), the address for California Avionics Laboratories Inc should read: 515B Westchester Dr. The address given is 515B Winchester Dr. The company has also changed its name to Cal-Av Labs.

Reader recalls remuneration for design

I cannot refrain from contributing my personal anecdote in support of Michael Markowitz's editorial (EDN, November 23, 1989, pg 47).

During the 1950s, I designed and then led the group in the development, production, and application phases of what I believe was the first transistorized digital airborne computer that was built in any significant quantity. As I recall, my salary at that time was approximately $10,000. Of course, in addition, I also received the customary $1 for each of the patents awarded in my name.

Perhaps I wouldn't have the time to write this letter except for the fact that I am another unemployed engineer attempting to live on limited savings.

Herbert E Miller, PE
Brookline, MA

A most refreshing breath of air

I rarely find the time to respond to something important that I've read, but Michael Markowitz's editorial, "Cut us in on profits, too" (EDN, November 23, 1989, pg 47), not only demands a response, but a resounding cheer!

All consumption must begin with innovation, and the first corporation to fully realize this "not-so-obvious" fact and to stick to a policy of paying the appropriate royalty for this service, will be the first company to demonstrate how fast their stock will climb to unbelievable heights. Engineers and scientists will be standing in line to produce better and better products for such a company. Other corporations, to survive, will soon follow. It is clearly the path for the future, just as much as π is a better constant to use than 3 in determining the area of a circle. In my opinion, respect for innovation through recognition and monetary rewards for both the corporation and the responsible innovator will do more to improve the quality of life on this planet than all other positive political and economic events combined.

Michael's editorial was the most refreshing breath of air that I've had since starting a career in engineering and could easily be recognized as one of the turning points in the future of this world. I hope to read more such editorials and articles that show cases where the shift toward individual recognition takes place. As more corporations take steps to protect their internal ideas and recognize responsible individuals, profits will be more readily retained, and immense growth will soon follow. Notice the effect when Intel decided not to license the 80386 microprocessor and the tremendous growth (more than 30% per month) experienced a few years ago when Ashton-Tate recognized Radcliff (author of DBase software) with more than $20 million dollars in royalties. If policies such as these not only continue, but become more focused on individual recognition, a "rush to innovate" will become more profound than any of the gold rushes ever experienced.

And I ask—who could be more deserving of these rewards? Engineers and scientists have given more to benefit civilization than any other class of society. I'm looking forward to a future extra rich in technology. In fact, we need it to survive. There is no doubt the payment of royalties for innovation is a vastly improved way to survive the future. Thanks for the vision and the willingness to comment on the reality of today and the prospects for tomorrow. My only regret is the inability to be here and watch how it changes in the next 100 years!

L F Smith
President
NW Silicon Specialists Inc
Portland, OR

Oops! Sorry, wrong number and address

On pg 96 of "EDN's 16th Annual µP/µC Chip Directory" (EDN, November 23, 1989, pg 92), the address and phone number for Fujitsu Microelectronics Inc are incorrect. The correct address and phone number are

Fujitsu Microelectronics Inc
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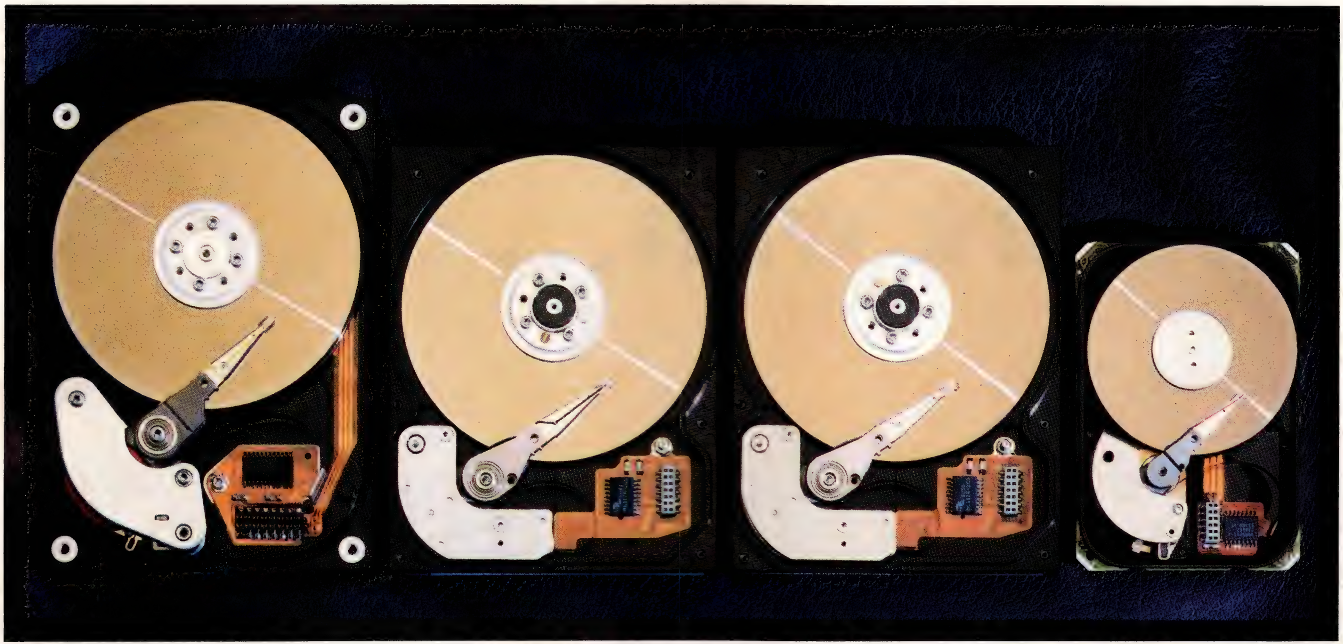

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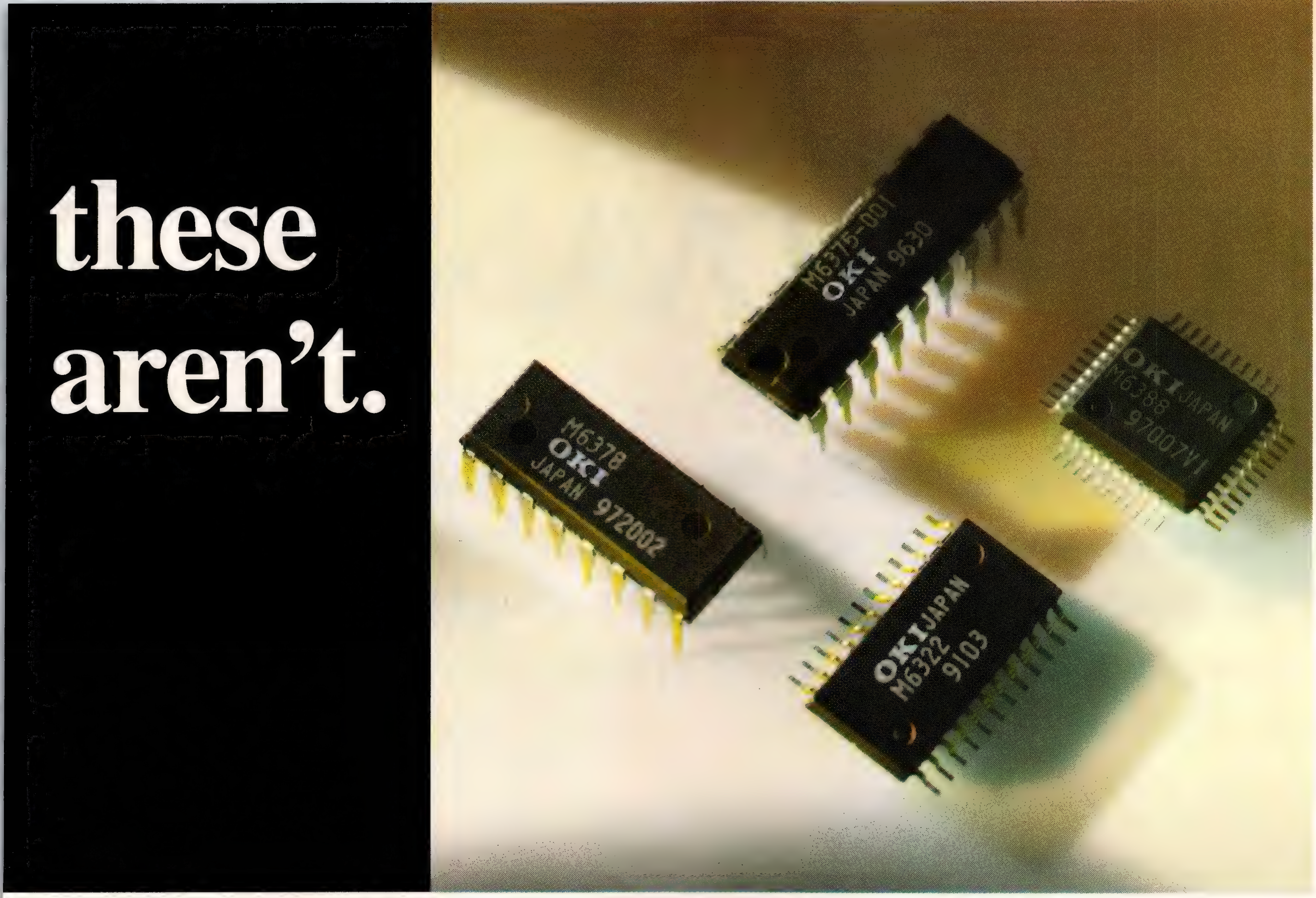

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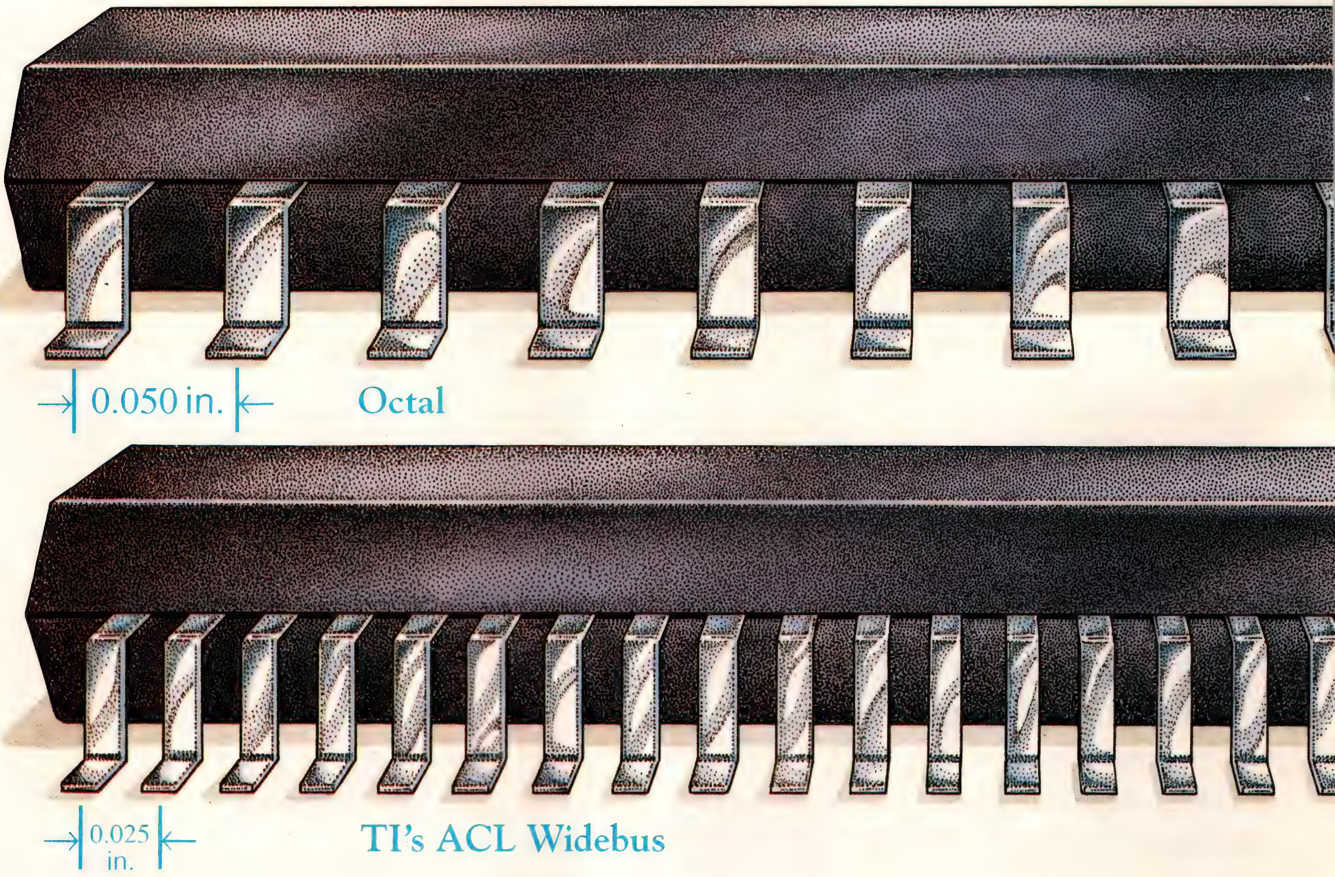
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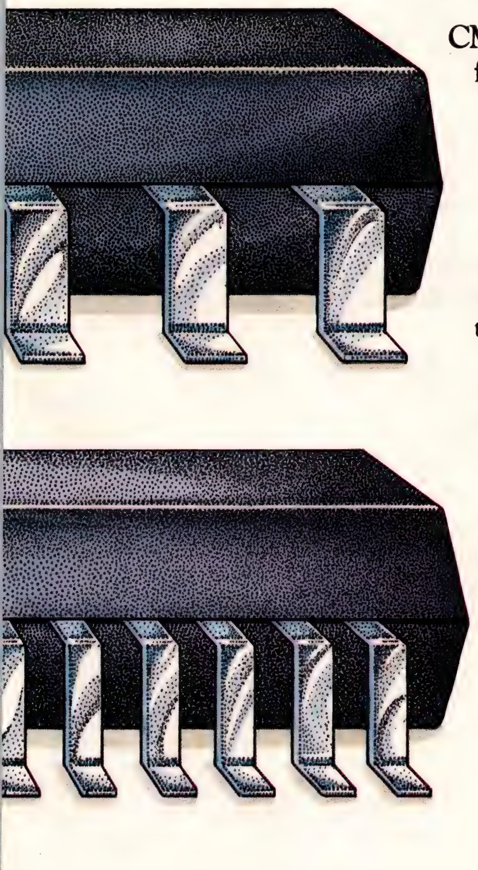

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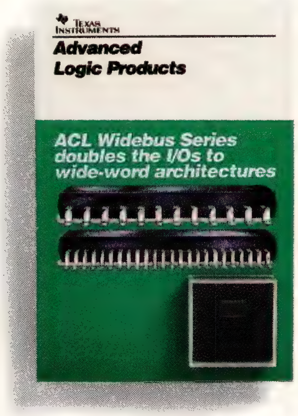
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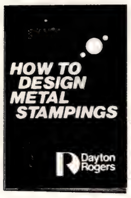

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CALENDAR

SECS Communications Seminar, San Jose, CA. GW Associates Inc, 1183 Bordeaux Dr, Suite 27, Sunnyvale, CA 94089. (408) 745-1844. February 26.

CASE: The Next Generation (conference), Boston, MA. Elaine Mershon, Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 475-6990. February 26 to 28.

International Conference on Design Automation Standards for Test, San Francisco, CA. Ronald Short, ADC Telecommunications Inc, 4900 W 78th St MS-74, Minneapolis, MN 55435. (612) 893-3247. February 26 to 28.

Compcon Spring '89, San Francisco, CA. Dr Kenichi Miura, Fujitsu America, 3055 Orchard Dr, San Jose, CA 95134. (408) 432-1300, ext 5408 or 5723. February 26 to March 1.

Spring National Design Engineering Show and Conference, Chicago, IL. Cahners Exposition Group, Customer Service, Box 3833, Stamford, CT 06905. (203) 964-0000. February 26 to March 1.

Electronic Imaging West, Pasadena, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126. In MA, (617) 232-3976. February 27 to March 1.

Nepcon West, Anaheim, CA. Cahners Exposition Group, Box 5060, Des Plaines, IL 60017. (312) 299-9311. February 27 to March 1.

Commercially Available Single-Board Computers and Real Time Operating Systems, Cambridge, MA. DSP Associates, 16 Peregrine Rd, Newton, MA 02159. (617) 964-3817. FAX 617-969-6689. March 5 to 8.

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ROM capacity	256K	512K	512K
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RAM capacity	512K	512K	512K
RAM supplied	512K DRAM	256K SRAM	256K SRAM
# Serial ports	2 RS232	2 RS232	2 RS232
# Parallel I/O	0	24 TTL	24 TTL
# Timers/# Bits	3 x 16-bit	3 x 16-bit	3 x 16-bit
Clock/Calendar	Yes	Yes	Yes
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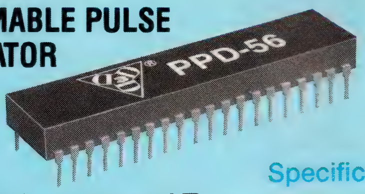

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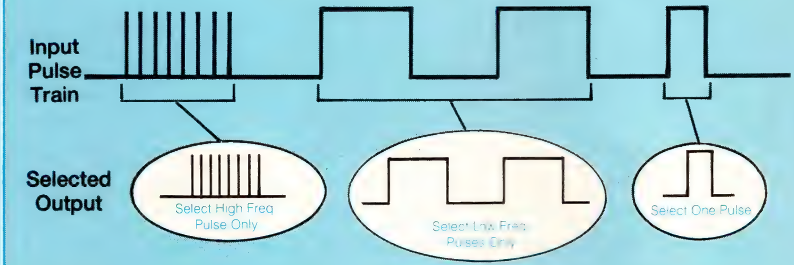

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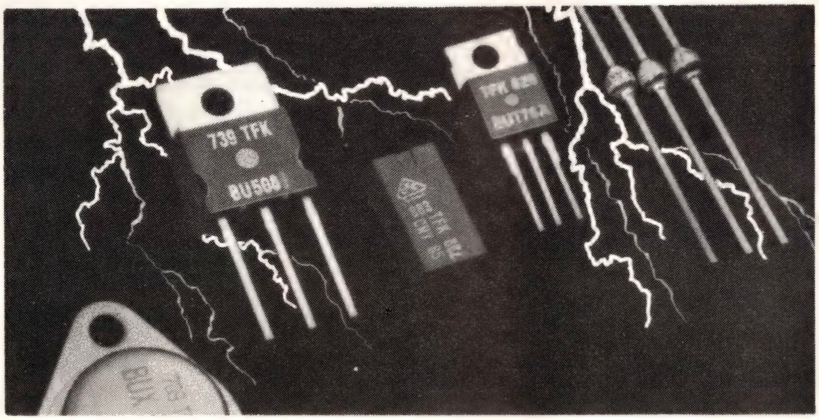

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CIRCLE NO. 6

CALENDAR

Designing for Electromagnetic Compatibility (short course), Mountain View, CA. Hewlett-Packard Co, Signal Analysis Div, 1212 Valley House Dr, Rohnert Park, CA 94928. (800) 247-3382. March 6 to 7.

Designing for Electromagnetic Compatibility (short course), Santa Clara, CA. Hewlett-Packard Co, Signal Analysis Div, 1212 Valley House Dr, Rohnert Park, CA 94928. (800) 247-3382. March 8 to 9.

The International Congress on Optical Science and Engineering/Exhibit, The Hague, The Netherlands. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX 206-647-1445. March 12 to 16.

Advances in Semiconductors and Superconductors: Physics Toward Device Application and Exhibit, San Diego, CA. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX 206-647-1445. March 17 to 21.

Professional Development Seminar, Houston, TX. USENIX Association, 5398 Manhattan Circle, Boulder, CO 80303. (303) 499-2600. FAX 303-499-2608. March 19.

Second Annual Oregon Workshop on Software Metrics, Portland, OR. Warren Harrison, The Oregon Center for Advanced Technology Education, Portland State University, Portland, OR 97207. (503) 725-3108. FAX 503-725-4882. March 19 to 20.

NCGA '90—Conference and Exposition, Anaheim, CA. NCGA '90, National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031. (800) 225-6242; in VA, (703) 698-9600. FAX 703-560-2752. March 19 to 22.

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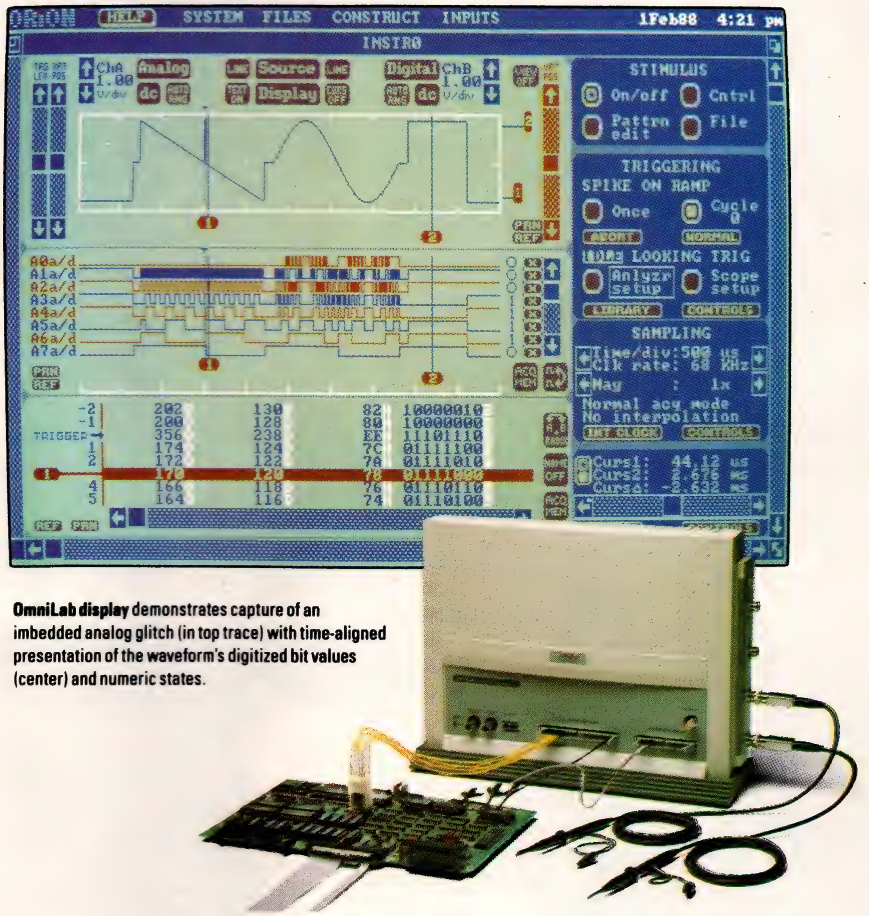
The 9240's general-purpose hardware allows you to configure and implement numerous application-specific instruments on the screen of your AT or PS/2, via simple pull-down menus. Then save the setups for future use. It's like having a benchtop of instruments in one.

- And with the 9240, you can troubleshoot in fewer steps than ever before—without compromising high performance specs. Result: you'll pinpoint faults faster and easier, get your designs to market quicker.



```
  -2   202   130   82  10000010
  -1   200   128   80  10000000
TRIGGER→ 356   238   EE  11101110
   1   174   124   7C  01111100
   2   172   122   7A  01111010
   1   170   120   78  01111000
   4   166   118   76  01110110
   5   164   116   74  01110100
```

```
Time/div:500 us
Clk rate: 68 KHz
Mag     :   1x
Normal acq mode
No interpolation
Curs1:  44.12 us
Curs2:  2.676 ms
CursΔ: -2.632 ms
```

OmniLab display demonstrates capture of an imbedded analog glitch (in top trace) with time-aligned presentation of the waveform's digitized bit values (center) and numeric states.

For more information, call **toll free 800/729-7700**
Or write for complete literature.

- Available for rent from U.S. Instrument Rentals, Inc., 800/824-2873

NO-COMPROMISE 9240 SPECIFICATIONS

DIGITAL OSCILLOSCOPE		LOGIC ANALYZER	
Digitizers:	Two, 8 bit	Inputs:	48, timing and state
Bandwidth:	100 MHz	Asynchronous Clocking:	34 MS/s on 48 inputs; 204 MS/s on 8 inputs
Single-Shot Digitizing:	34 S/s to 204 MS/s		
Repetitive Sampling:	680 MS/s	Repetitive Sampling:	680 MS/s on 48 inputs
Scale Factor:	10 mV/div to 10V/div in 1-2-5 sequence	Synchronous Clocking:	0 to 34 MS/s
		Acquisition Memory:	4K samples (16K optional)
Record Length:	4K (16K optional)	Disassembly Options:	Over 33 microprocessors
ANALOG STIMULUS		**DIGITAL STIMULUS**	
Output:	8mV to 8 V peak-to-peak, 8 bit	Outputs:	24, 74F tri-state drivers
Cycle Length:	4 to 4K samples (16K optional)	Cycle Length:	4 to 4K samples (16K optional)
Clocking:	34 S/s to 34 MS/s	Timing:	34S/s to 34MS/s
Functions:	Record, edit and playback	Functions:	Record, edit and playback

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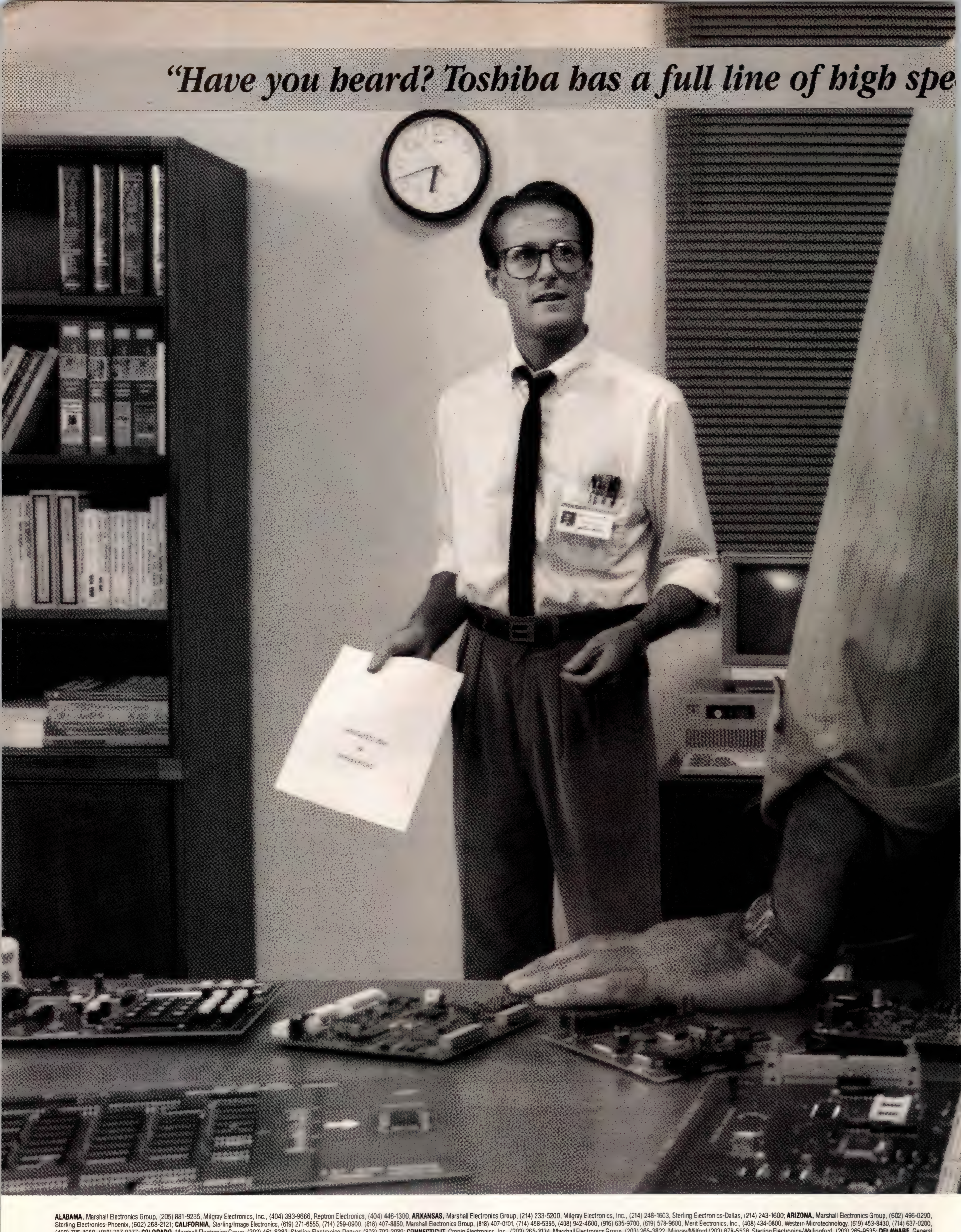
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Toshiba High-Speed SRAMs

Configuration	Density	Speed (ns)				Availability
64K x 1	64K	35	45	55		Now
16K x 4	64K	15	20	25	35	Now
16K x 4 (OE)	64K	15	20	25	35	Now
8K x 8	64K	15	20	25		Now
8K x 9	72K	15	20	25		Now
4K x 18 x 2	144K	20	25	30		Now
8K x 18	144K	20	25	30		Now
64K x 4	256K	17	20	25	35	Now
64K x 4 (OE)	256K	17	20	25	35	Now
32K x 8	256K	17	20	25	35	Now
32K x 9	288K	17	20	25	35	Now
16K x 12	192K module	25	35			Now
16K x 16	256K module	25	35			Now

PART	$\overline{CE}$	A12	t_{acc}	t_{OE}	V_{cc}	PACKAGE
TC55187	unlatched	unlatched	20/25/30	10/10/12	± 10%	PLCC
TC55188	latched	latched	20/25/30	10/10/12	± 10%	PLCC

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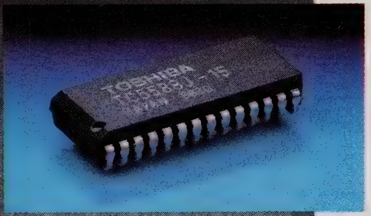

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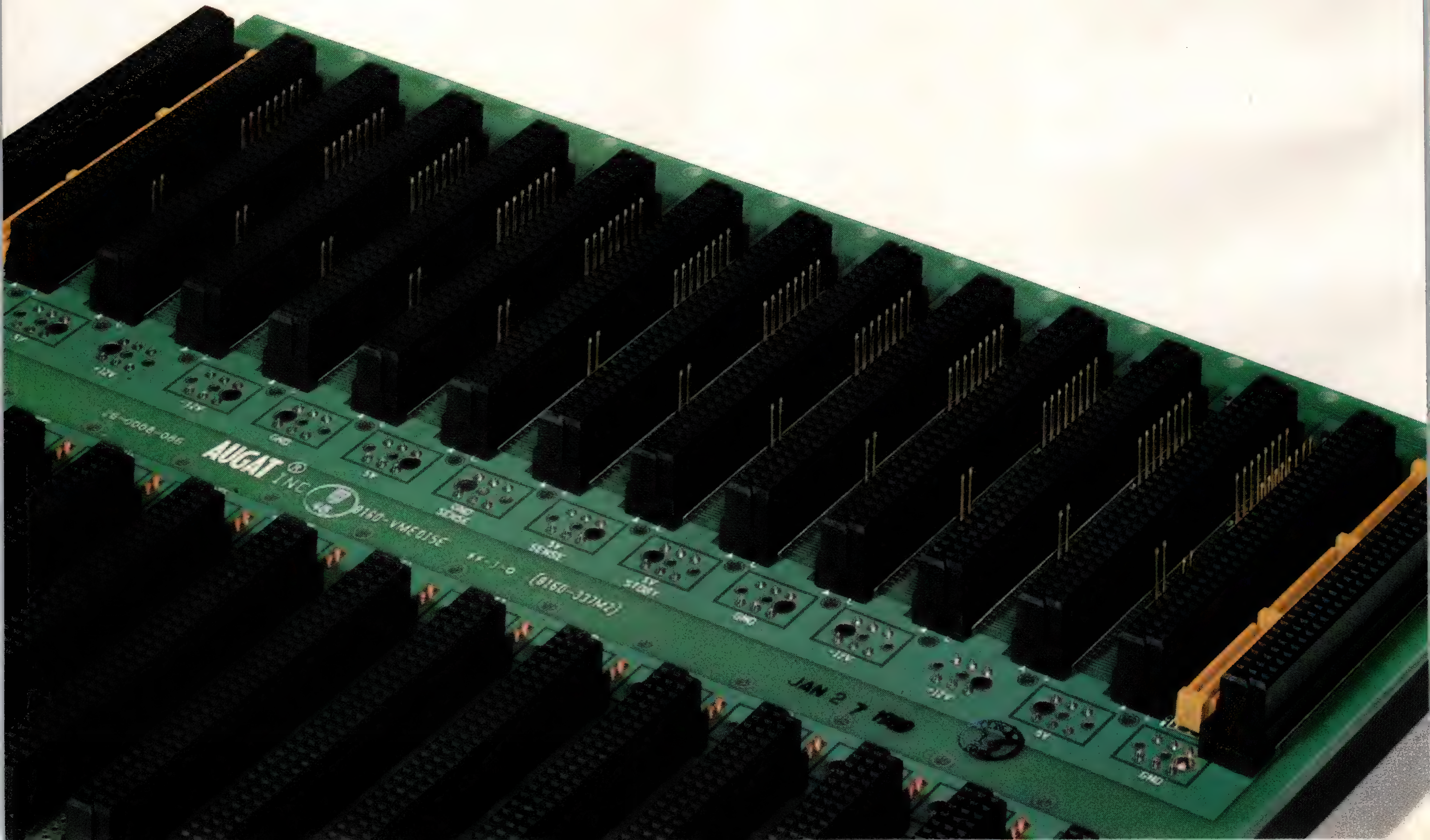

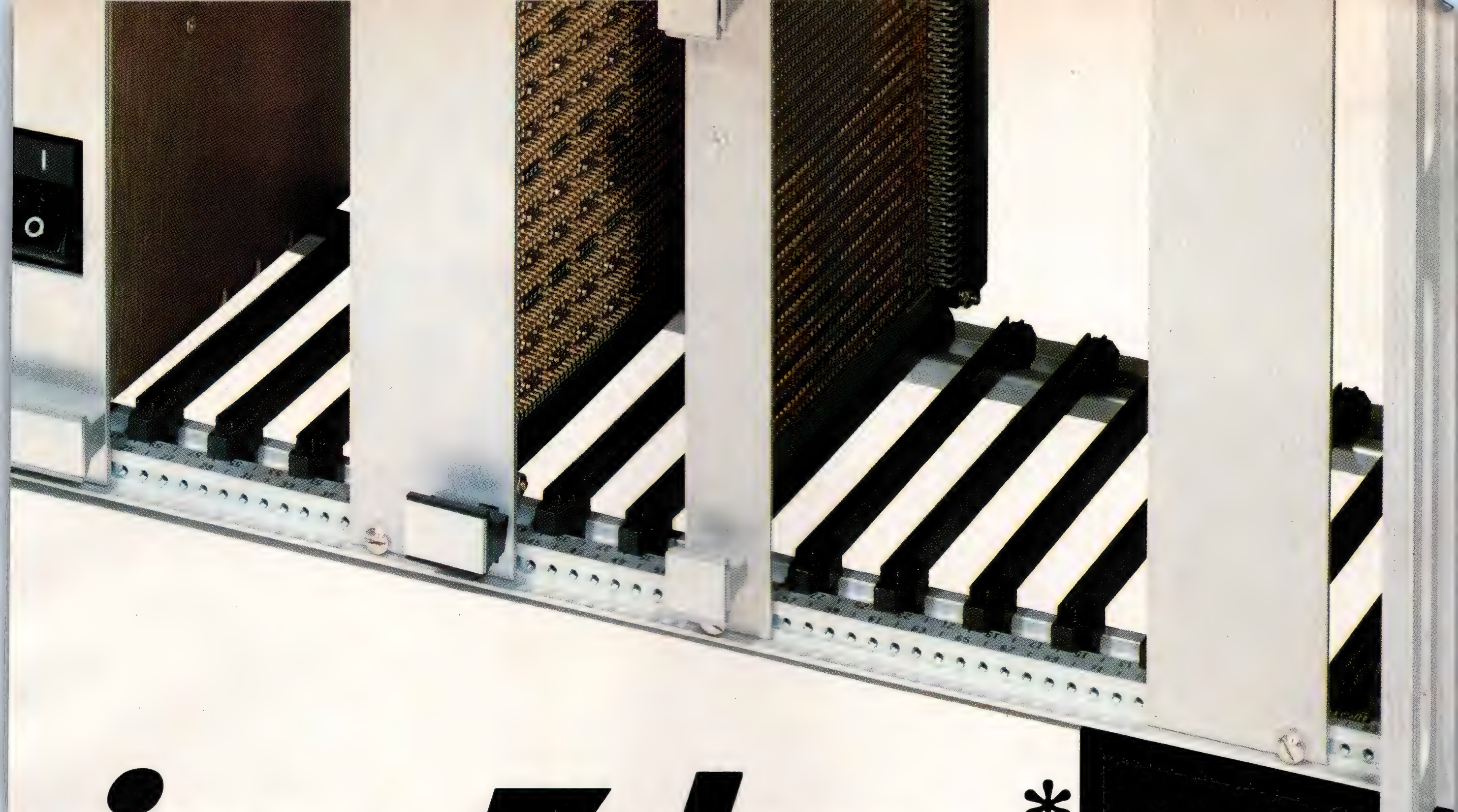

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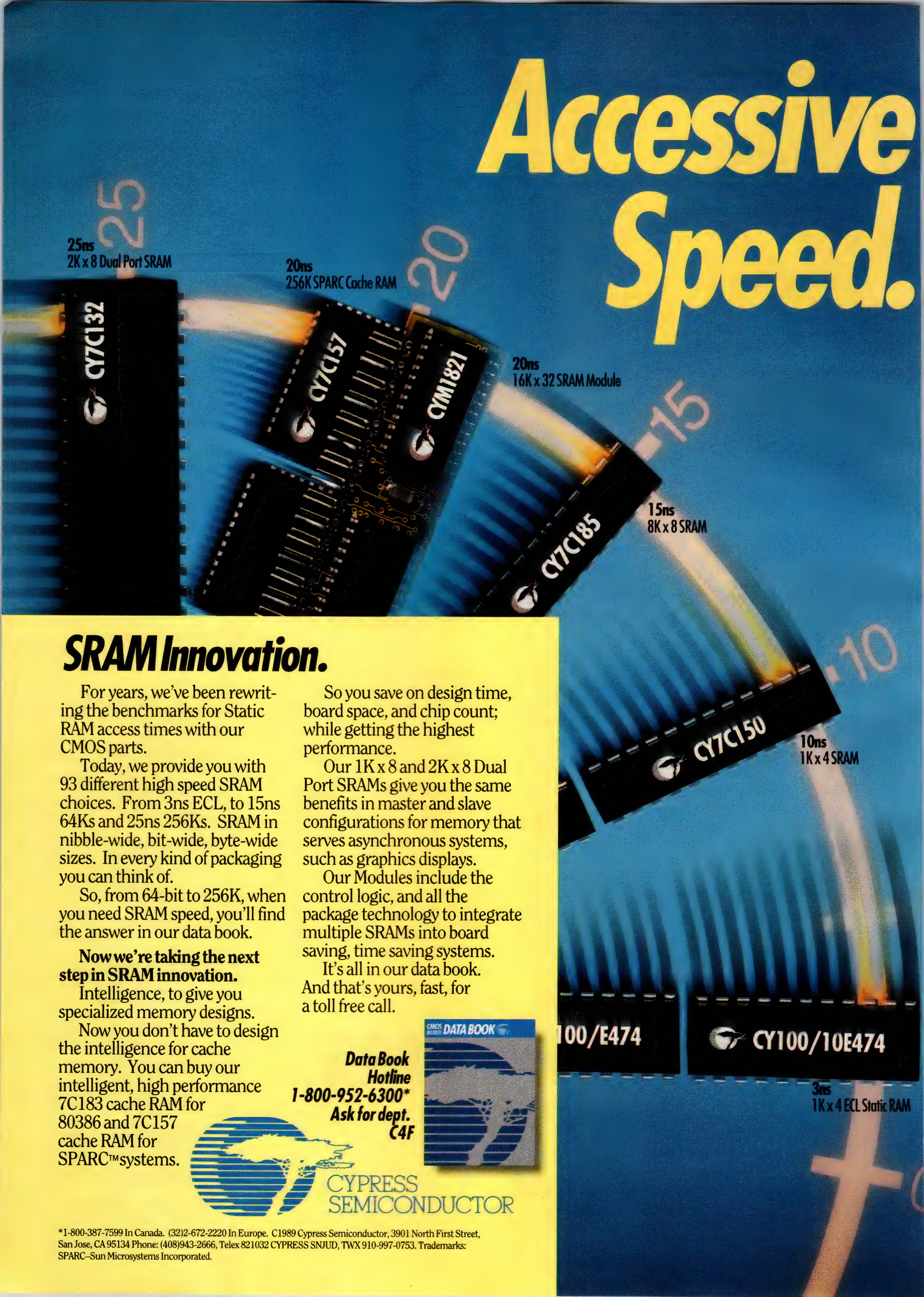

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EDITORIAL

Quality is its own reward

A great deal of fuss is being made over the Malcolm Baldridge National Quality Awards program, which was set up by Congress in 1987. Among the several companies that have won the award are Motorola and Xerox Corporation's Business Products and Systems Division. I am pleased to salute all the companies that have won a Baldridge award, but I'm also wondering whether some applicants aren't more concerned about winning the award than about what should be the real goal—high quality.

Applying for the award isn't a trivial task; the guidelines and forms for the 1989 awards take up 40 pages. Companies respond to essay questions in examination categories such as customer satisfaction, quality results, human-resources utilization, and leadership, and they receive points for their answers. Those exam answers require much research and preparation. According to the *Wall Street Journal*, an award team at Corning Inc spent 7000 person-hours on the award application and exam answers. Likewise, Xerox budgeted $800,000—not including salaries for 20 full-time staff people—for its application. The company submitted 251 loose-leaf binders of exam answers and supporting information. The use of time, talent, and money doesn't stop with the submission. During the final judging, the awards committee visits plant sites, interviews people in the company, and reviews facts and figures—all at the applicant's expense.

I'm sure that some companies use the award's examination steps as a way to appraise their quality efforts, review customer relations, and develop new leadership plans. But I'll bet that other companies simply want to win the award so that they can use it in advertising to tout their claims of quality supremacy. Of course, this tactic assumes that the company's customers know and care about the award.

In the rush to win quality awards, some of us have forgotten that high quality is its own reward. By adopting a program that sets, monitors, and raises goals for high quality—and rewards quality performance—a company and its customers, shareholders, and employees are all winners. If I had $800,000, I wouldn't spend it on a one-shot award. Instead, I'd invest it in a continuous internal quality-assurance program that would let my customers be the final judges. In today's competitive world, that's really all that counts.

Jon Titus

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975
American Society of
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1988, 1983, 1981

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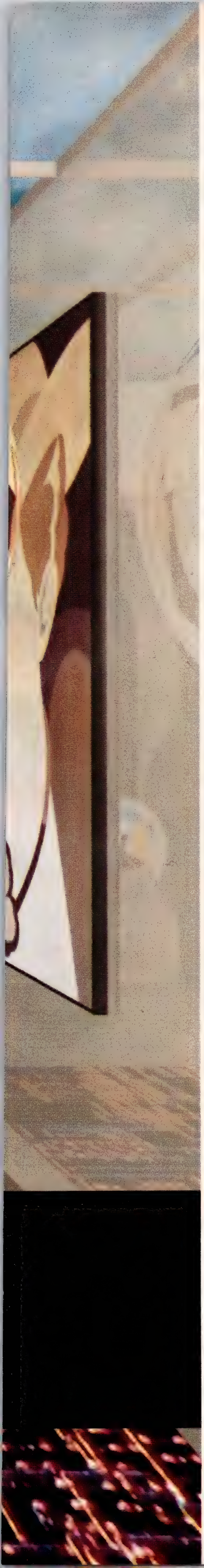

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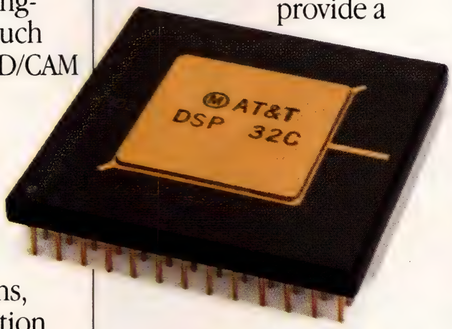

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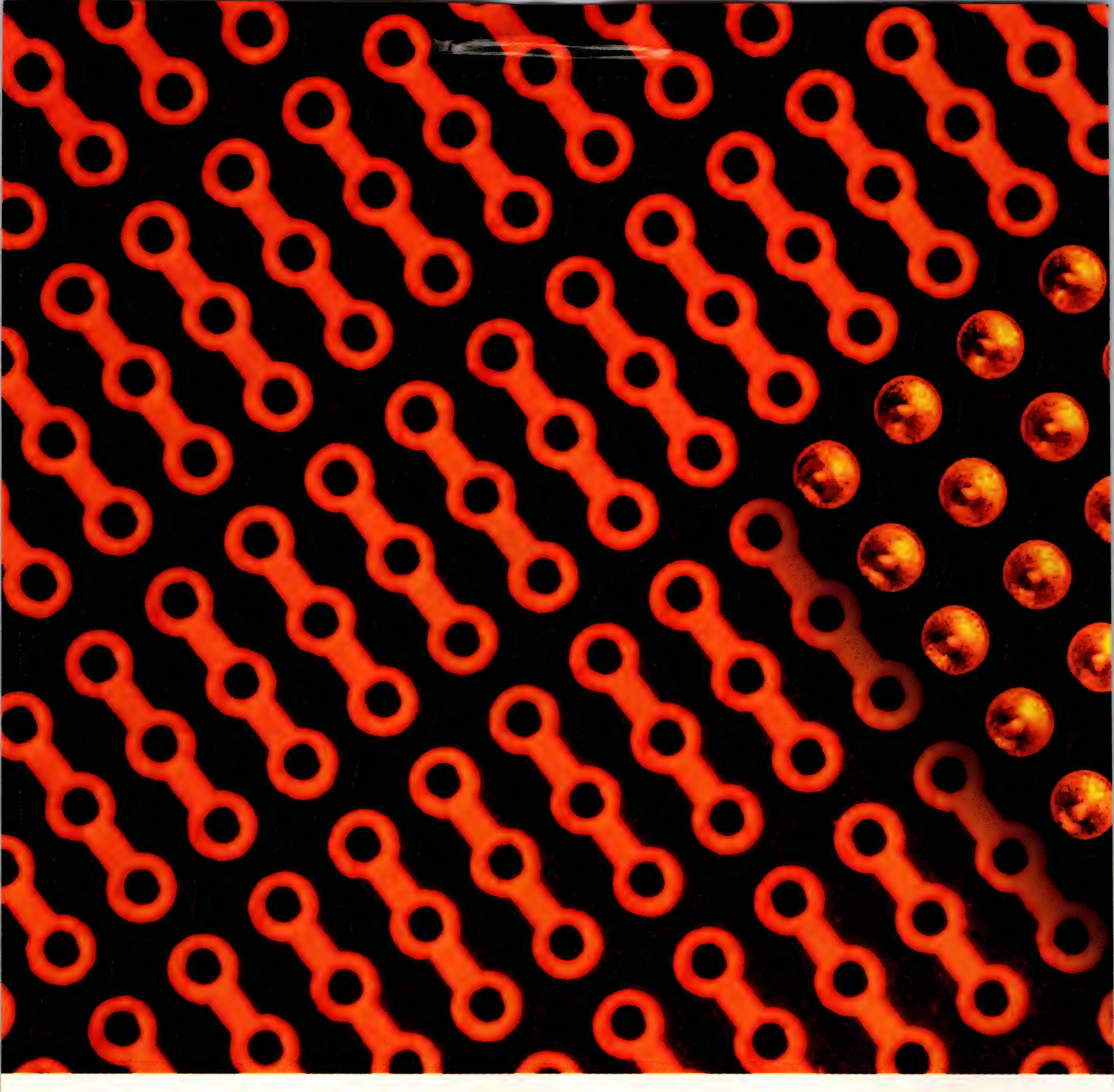
The right choice.



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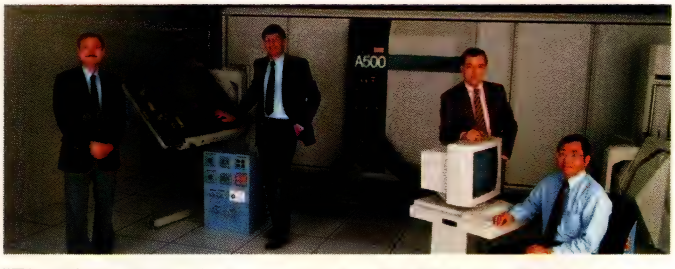

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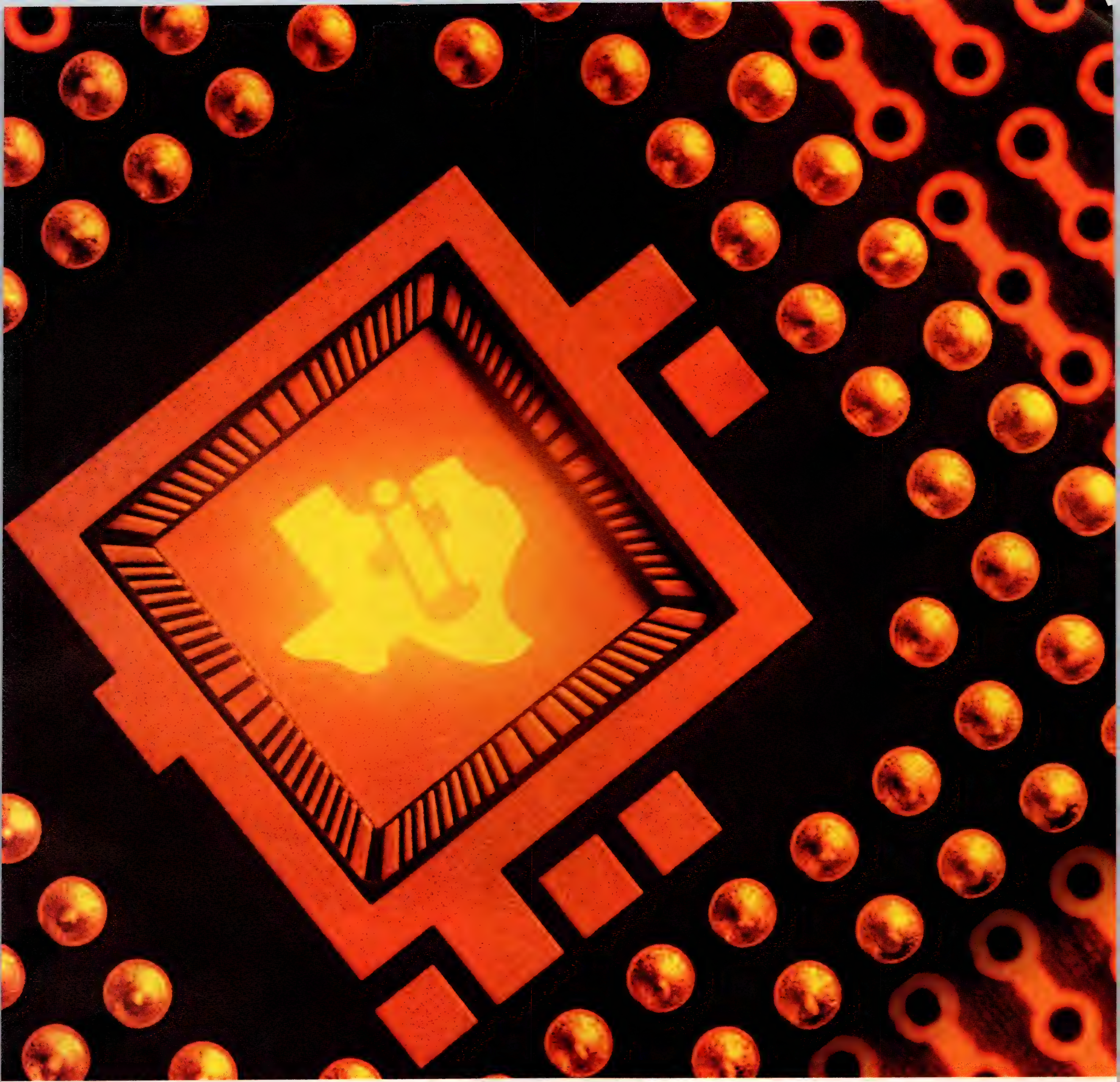

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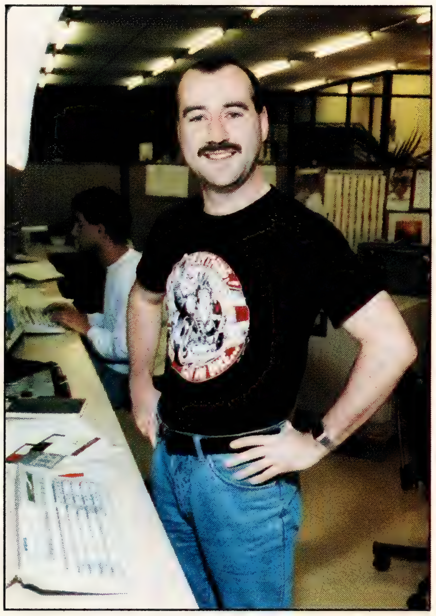
Modern spirit, traditional reserve:

The character of a British electronics company

Article and photographs by Gary Legg,
Special Projects Editor

This article is the second in an occasional series about engineering in Europe.

The ceremony at the St Albans headquarters of Marconi Instruments is very, very British. The Mayor and Mayoress of St Albans, a small city about 30 miles north of London, sit in the first row. On stage is the Lord Lieutenant of Hertfordshire, the county representative of Her Majesty the Queen. Resplendent in medals, epaulets, and sword, the Lord Lieutenant reads a scroll from the Queen recognizing Marconi for technological achievement in developing the Model 2955 mobile radio test set. Afterwards, there is a high tea.


Marconi software engineer Steve Thomas is comfortable in his typical work attire.

A few miles away, in the engineering lab at Marconi's facility in Stevenage, the scene is less ceremonious. Scopes, logic analyzers, and in-circuit emulators top workbenches; posters, charts, and an occasional nudie calendar decorate the walls. Virtually all of the site's 300 or so workers are casually dressed, and almost every engineer in the lab wears jeans. One is in shorts and sandals. On the T-shirt worn by Steve Thomas, a software engineer, is a cartoon of a cheeky motorcyclist proclaiming, "Stuff everything! I've always got my bike."

Bold versus old

Thomas's T-shirt and the Lord Lieutenant's regalia are symbols of a British dichotomy in which contemporary audacity conflicts with, and yet rather peacefully coexists with, traditional reserve. In newspapers, the scandalous Sun and the equally scandalous Star compete with the staid Times of London. In fashion, it's the punkers and Saville Row. At Marconi, as in England in general, fresh informality coincides with centuries-old ceremony and decorum.

Sometimes, however, new notions don't easily coexist with tradition. For example, many engineers at Marconi express distaste for practices that they see becoming more-or-less standard contemporary marketing procedures for many of the world's electronics companies: fudging published specs, rushing products to market before they're ready, and bidding "creatively" on defense contracts. Some Marconi engineers give the impression that British integrity—part of a larger tradition of overall civility, which is still noticeably present in England—precludes their resorting to such activities themselves.

Marconi engineers' may not base their disapproval of such tactics solely on traditional propriety, however. Marconi is primarily an exporting company and thus directly competes with many companies, particularly in the US, that its engineers criticize. Only 10% of the world instrument market is in the UK, and Marconi exports almost

"Beefeater" guard at the Tower of London.

"The Americans wanted us to sell it before we finished designing it. That is totally alien to us."

Development Manager Paul McAllister is an ardent foe of "specsmanship."

70% of the instruments it produces.

"Specsmanship"—writing product specifications that are misleading—is the target of much criticism by Marconi engineers. One particularly disturbing aspect of it, according to some engineers, is the listing of performance specifications that companies don't validate with testing. "In most cases," claims David Owen, projects manager for Marconi's Radio Communications Group, "they don't actually carry out the tests at all." In one case, he says, an American instrument that Marconi "factored" (imported and sold under its own name) often failed to meet its published specifications when used in the field. Marconi temporarily withdrew faulty units from the market and reworked them.

Paul McAllister, development manager for Marconi's Sources and Analysers Division, disagrees with Owen on the degree to which testing to validate specs goes undone. "They carry out some of the tests," he says of suspect companies. "They pay lip service." But, McAllister says, American companies are often "much more keen to get things to the market. If they're confident of the thing, they'll not do the test. If they haven't got the time, they'll say, 'Right, we'll take a flyer on it.' There's just no way in our company cultural structure you could do that."

Unsupported claims about product performance often revolve around the word "typical," according to McAllister. "We have a definition of typical," he says, "and so do the Americans. They're different. Our definition of typical is that 95% of all units will meet it and that [our production department] will produce statistical evidence to back it up. That is an enormous overhead in production and money."

"Some American companies," the outspoken McAllister continues, "will sample-test a few [units] and just say this is typical performance without saying what percentage. The more honest ones of them, like HP, will split their spec into warranty performance, which is about five items, and about three pages of nonwarranty performance, which are all the 'typical' results." Perceiving a competitive advantage to this practice, Marconi is reevaluating its policies. "I think ultimately we'll go the way HP has gone and go for warranted and supplemental characteristics," McAllister says.

Marconi engineers don't seem overly resentful about American marketing practices, just bemused and preferring to stick to their own traditional ways. When working with an American company on the possibility of developing a product jointly, they were surprised, according to McAllister, that the Americans "wanted us to sell it before we finished designing it." Similarly, Marconi was surprised when the same American company suggested bidding for a military contract that would provide product-development funds before a design was known to work or even existed on paper. "That is totally alien to us," McAllister says.

Owen notes, however, that even within Marconi there is pressure to get a product to market before it's ready. The selling prices of instruments are on a downward trend, he says, but development costs keep going up. Early market entry is not only a competitive advantage but also generates much-needed early revenue to offset those costs.

Still, Marconi's trip to market isn't exactly a mad dash. According to Sandy Warwick, Marconi Instruments' director and general manager, developing a new instrument takes at least two or three years and has been known to take seven. In developing the recently introduced 2030 series signal generators, for example, the company scrapped two designs before proceeding with a third. Nevertheless, the final design did facilitate on early market entry. By simplifying the range of products in the series, it speeded up development of the first product, the 2031.

Malcolm Evely, the 27-year-old project leader who took over the 2030 series when 21-year-veteran Owen received a promotion, reflects the relaxed pace at Marconi. "The commercial pressure is on to get things done," he says, "but we do have a management structure that buffers us slightly from that. It's a nice environment to work in."

It's also a casual, almost nonchalant, environment—surprising to anyone expecting British formality. Wearing shorts and sandals on a cold, dreary day, Evely probes a circuit board in a signal generator marked "Victoria" on its front panel with plastic tape. (The six 2031 development units, Evely explains, are named Albert, Bailey, Cuthbert, Dougal, Victoria, and Number Six.) Evely wears shorts to work, he says, because he feels uncomfortably warm at the temperature preferred by his coworkers. "No one's complained yet," he says of his attire, but then he reconsiders: "Well, I take that back," he says with a wry smile. "Some of the ladies in production have complained."

Owen, Evely's boss, dresses casually himself, although his slacks and open-necked white shirt tend to set him apart from most of the jeans-clad engineers. "It doesn't really matter what you look like," he says. "If we're going out on a visit, we wear a suit. If we're just working in the lab here, we may as well wear what we bloody like."

Owen's desk, set in the middle of a large bay containing other desks and workbenches, hints at both hard work and play. Papers cover most of its surface, and a small rubber duck sits on its edge. Marconi teammates gave him the toy last summer, Owen explains, after a "duck" in cricket—an event seemingly impossible to explain to someone versed in baseball, but apparently somewhat akin to striking out on a wild pitch and leaving runners on base.

Throughout the rest of the lab, the mood and the decor are also cas-

John Wells: Wizard without a plan

"I've never viewed what I do in any sense as being a career. It's just pursuing an interest; it's just doing something I like doing."

So says John Wells, 38-year-old senior principal engineer and acclaimed technical wizard at Marconi Instruments in Stevenage, England. Wells's career hasn't gone according to plan for the simple fact that there hasn't been a plan. But until he comes up with one, Marconi will gladly support him in his noncareer. They'll also gladly pay him more money than many of the company's managers make.

Wells is the beneficiary of a Marconi policy to reward technical ability as much as management skills. He also benefits from an attitude that allows and encourages engineers to do what they do best. In the case of Wells, that's design—outstanding design—without the necessity of management tasks and with few requirements to interface with others.

Typically, Wells takes on one-man projects: He gets interested in a problem, goes off by himself for a few months to work on it, and then comes back with the result. Almost invariably, the result is an elegant and eminently reliable design. "John will come up with actual circuits and layouts, and they will work," says Marconi Development Manager Paul McAllister, "And you will not have problems with them, tolerances or otherwise."

The most recent masterpiece from Wells is the synthesizer for Marconi's 2031 signal generator. It was especially gratifying to see the design work, Wells says, because "a number of eminent people within the Marconi empire" told him it wouldn't.

"They told me the whole technique was fundamentally flawed," Wells says, "but because I had absolutely no preconceived ideas that the technique shouldn't work, it didn't stop me getting it working. It was a bit like the bumble bee, really. In theory, it shouldn't be able to fly. But look at it. The bumble bee doesn't actually know that. The bumble bee can fly perfectly well."

What's next for Wells? "I just take whatever opportunity appears best as I go along," he says. "I figure if you try and plan too far ahead, you're bound to come unstuck anyway."

Marconi's is a casual environment, surprising to anyone expecting British formality.

Projects Manager David Owen shares a desk with a duck, a booby prize from cricket teammates.

ual. No one has complained about the scattered girlie calendars in the engineering department, Owen says. But then he notes that there are no women engineers at the site. In the production department, one or two women have posted their own beefcake pin-ups.

Contentment with the relaxed and relatively pressure-free work environment in British electronics companies may be one reason why few engineers there choose the intense pressure and risks of entrepreneurial ventures. Few small companies provide even basic engineering services such as circuit-board layout; large companies provide whole ranges of services in-house.

Other factors are probably more constraining to would-be entrepreneurs, however. For example, venture capital is difficult to obtain—the British seem not to have a proclivity for risk-taking. In addition, the electronics industry in the UK is dominated by domestic sales to the military and government agencies and by exports, all of which favor larger companies. Start-ups, according to Owen, are more likely to be nontechnical ventures and are more apt to be started by accountants than by engineers.

The accounting profession, in fact, is wooing some British engineers away from technical work with opportunities to earn higher salaries. Development Manager McAllister cites the case of a Marconi engineer with a doctorate and five or six years of experience who makes less than his wife, an accountant for only two or three years. England has the most accountants per capita in the world, McAllister says, "And God only knows why. They only count what happens."

Typical salaries for electronics engineers near London with five years of experience range from around £16,000 to £22,000 (about $26,000 to $36,000). Benefits are generally good, however, except when compared with those offered by companies on the European continent. Asked about vacation time, for example, McAllister responds, "Oh, it's quite low—25 days plus public holidays." The five weeks of vacation applies to beginning engineers as well as veterans; there is no increase with seniority.

Relatively high living costs accompany British engineers' modest salaries. A 3-bedroom "semi-detached" (duplex) dwelling near the Marconi sites north of London costs £100,000 to £150,000 (about $163,000 to $244,000). The area's proximity to London contributes to the high prices. Prices are higher yet in the city, but lower farther out.

High tech on the heath

Still, British engineers—or engineers at Marconi, at least—seem fairly content. Their work is state-of-the-art and challenging, and their environment is relaxed, both on the job and off. St Albans and Stevenage, sites of Marconi facilities, are quiet towns that contrast sharply with many American high-tech concentrations. Between them are rolling green hills gridded with English country lanes, many wide enough for only one car.

Within this setting, near the bustle of London but not a part of it, Paul McAllister sums up his view of British engineers in the world at large. The Americans will get a product to market first, he says, and the Japanese will production-engineer it better, but British design quality is generally superior. "If there's an elegant solution," McAllister says, "we usually find it."

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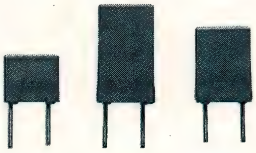

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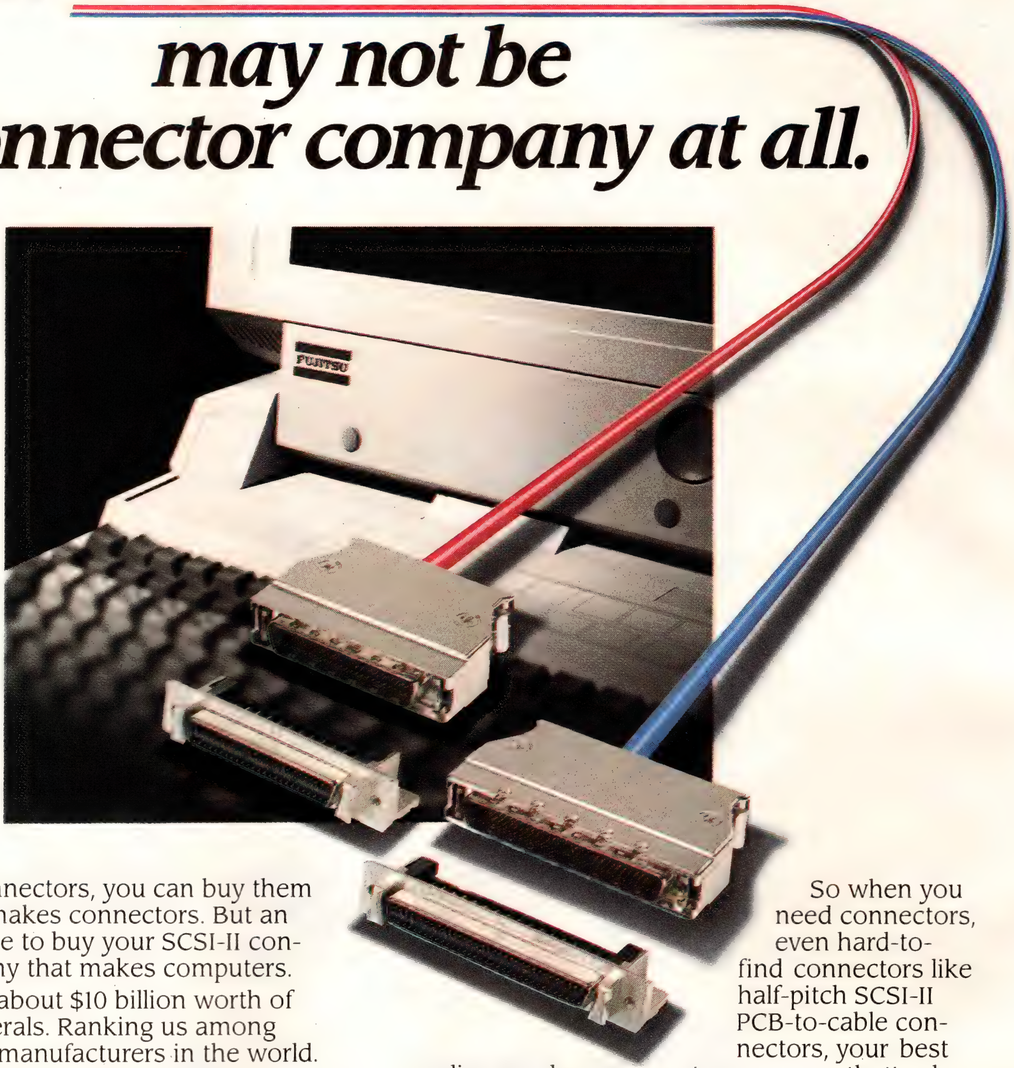

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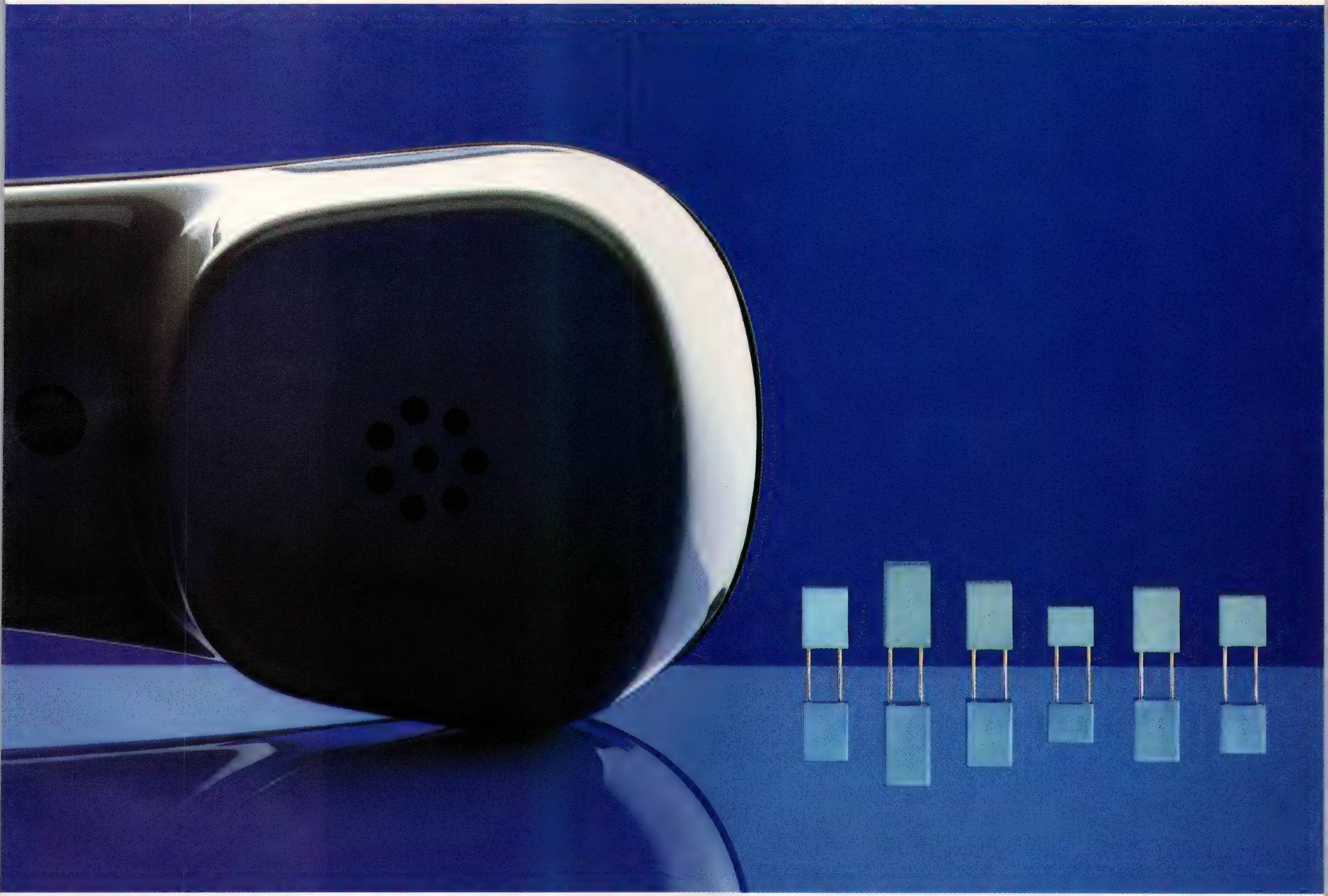

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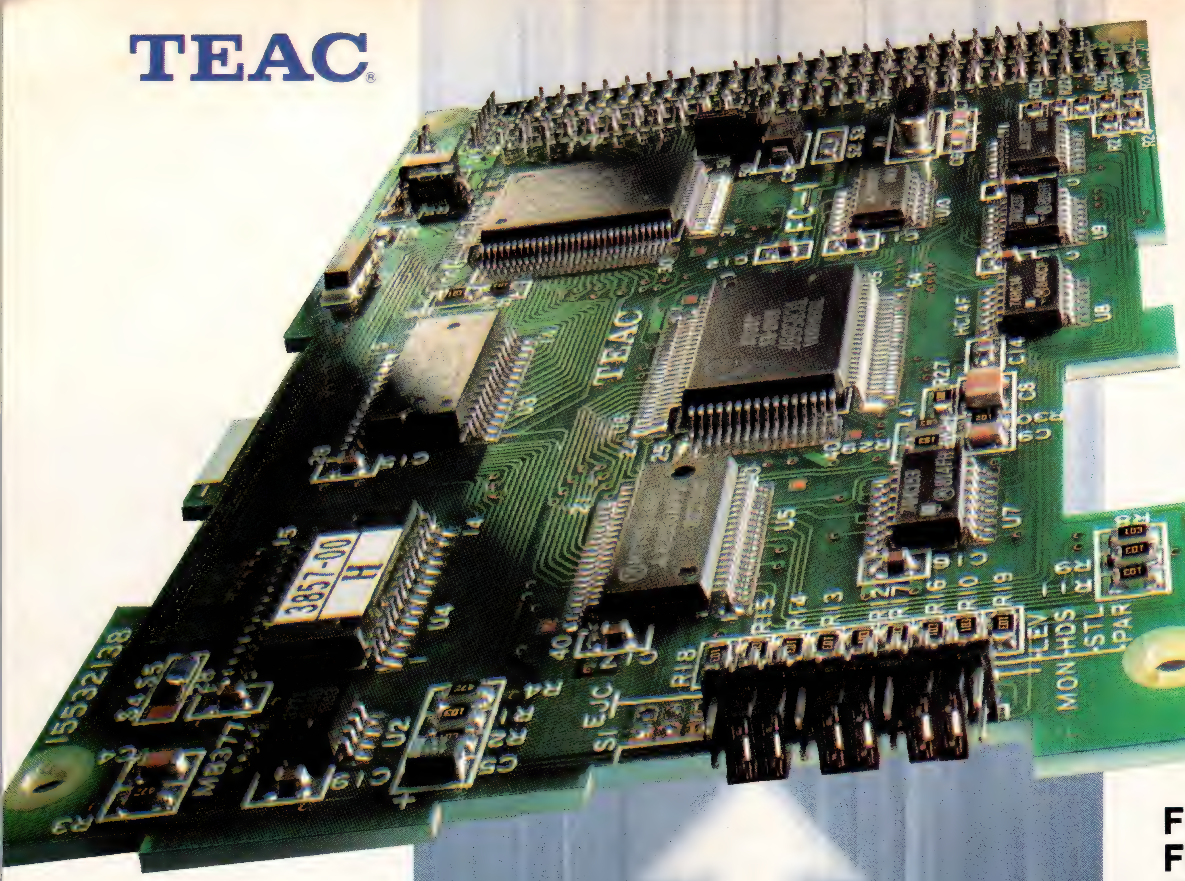

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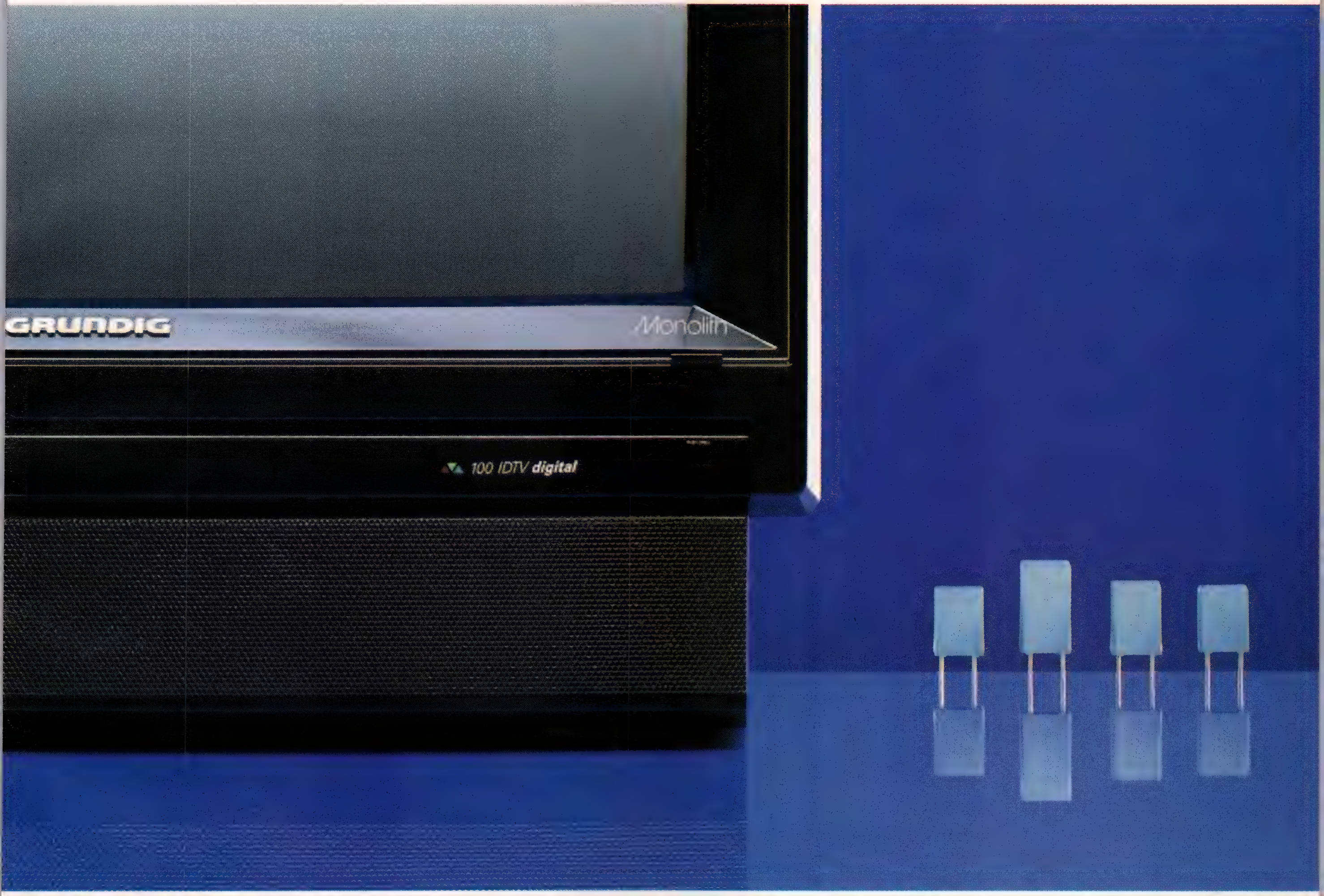

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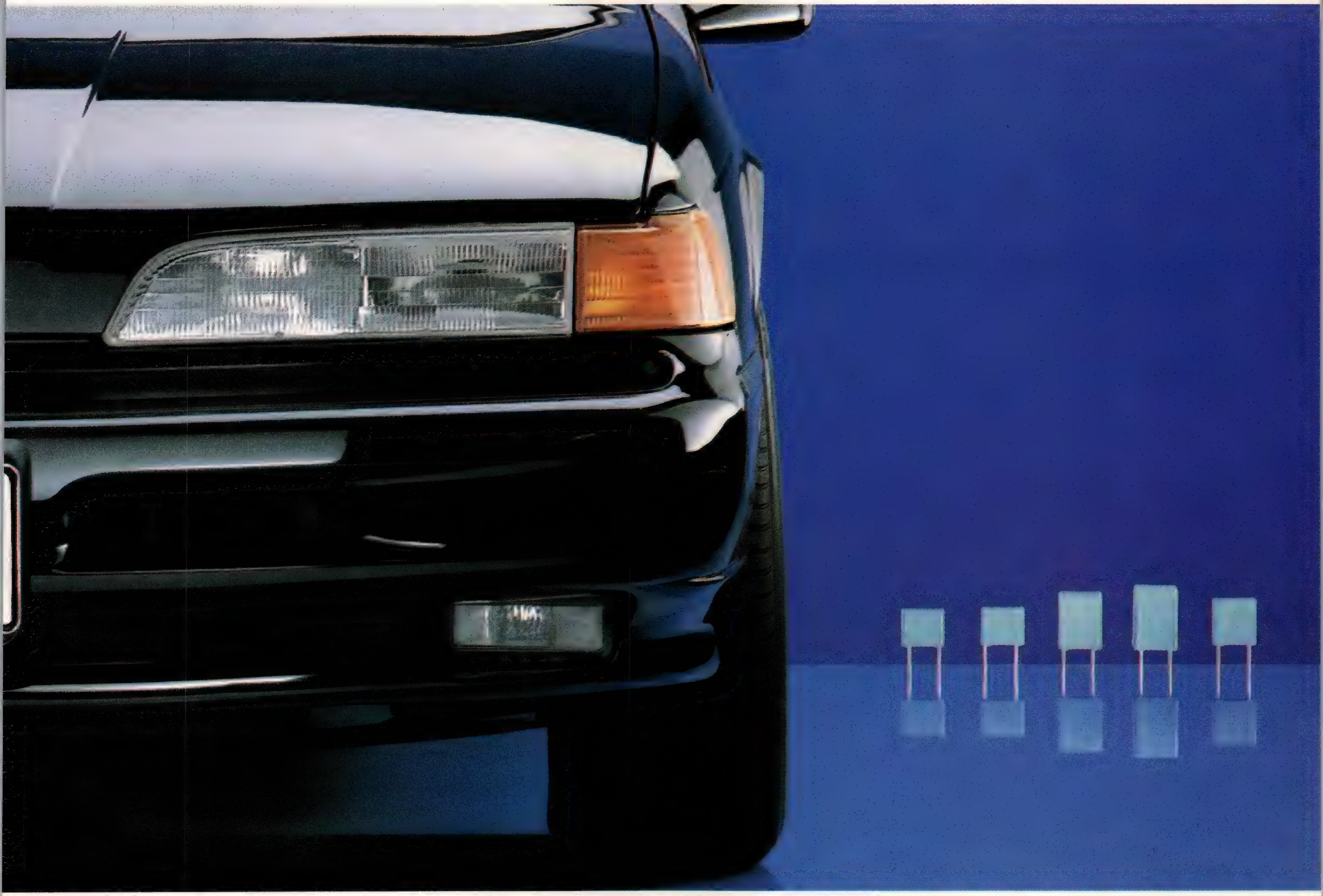

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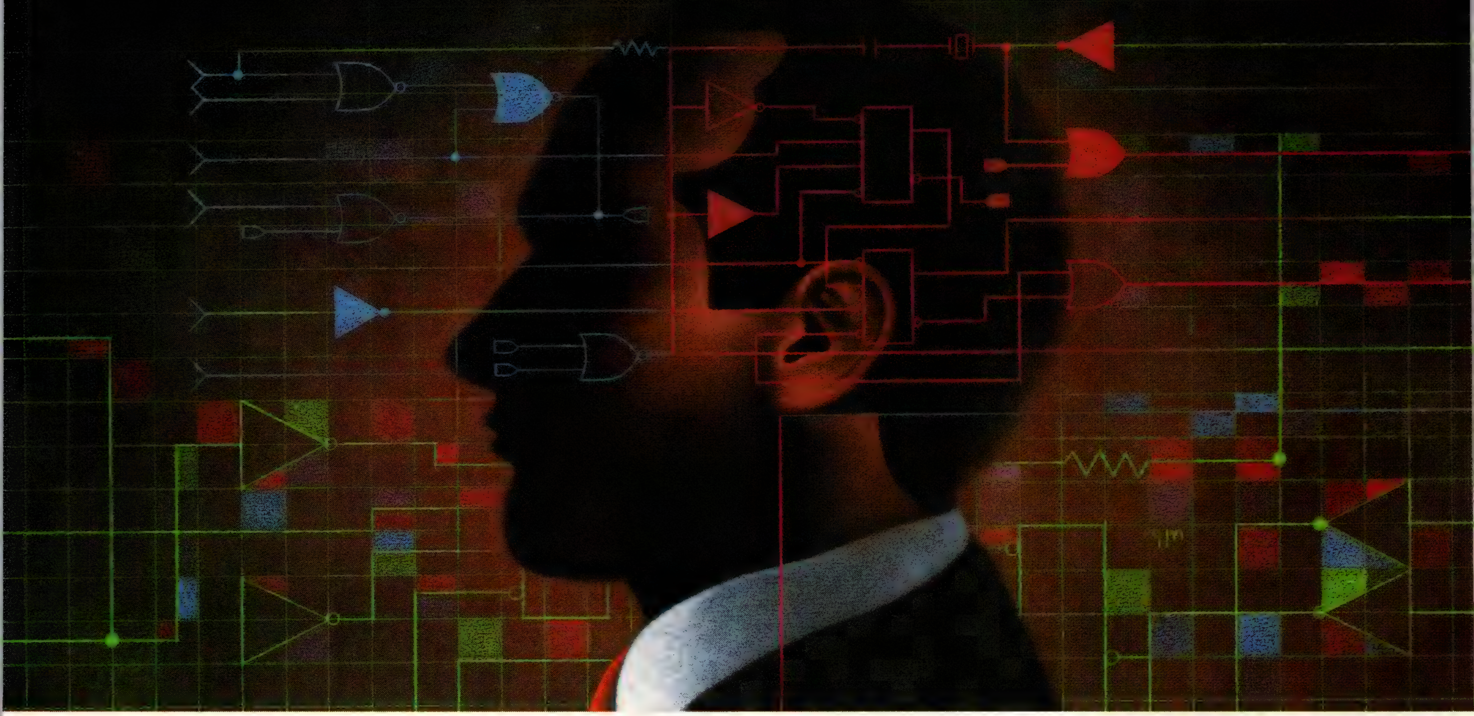

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Infrared-radiation thermometry accrues the many benefits of noncontact temperature measurement. One of the most important benefits of this type of measurement is that, by detecting only the IR energy emitted by a hot body, the temperature reading reflects the localized temperature of the radiant body and not the ambient temperature of the surrounding medium. Therefore, IR-radiation thermometers can monitor the temperature of hot spots, small targets, and moving bodies more accurately than contact devices, which respond to ambient temperature. In addition, because the IR-radiation temperature probe doesn't contact the radiant target, it doesn't damage fragile bodies.

Unlike IR-radiation thermometers, thermocouples and resistance temperature devices must come in contact with either the hot body or the surrounding medium. These transducers measure heat via conduction or convection, so they respond to the temperature of their surroundings, which may be different from the temperature of the target. Another disadvantage of contact sensors is that they can damage fragile bodies.

IR-radiation detectors have shorter thermal time constants than contact sensors. IR-radiation detectors have thermal time constants of a few hundred milliseconds, whereas thermocouples and resistance temperature detectors have thermal time constants of several seconds. Because they have faster time constants, IR-radiation thermometers respond more quickly to temperature variations in the target and give accurate readings for moving objects with wide temperature ranges.

Noncontact temperature probes cost almost ten times more than contact probes, but their ability to perform precise temperature measurements can reduce the cost of process control. IR-radiation thermometers contain an optical section that focuses the radiant energy from a target onto the detector. Detectors located 20 cm away from the heated body can detect radiant energy from a target a few square millimeters in size. This capability lets IR-radiation thermometers measure the temperature of

Dual-wavelength thermometers are insensitive to emissivity variations. *Williamson's Tempmatic 8000 Series measures temperature by computing the ratio of IR energy in two adjacent wavelength bands.*

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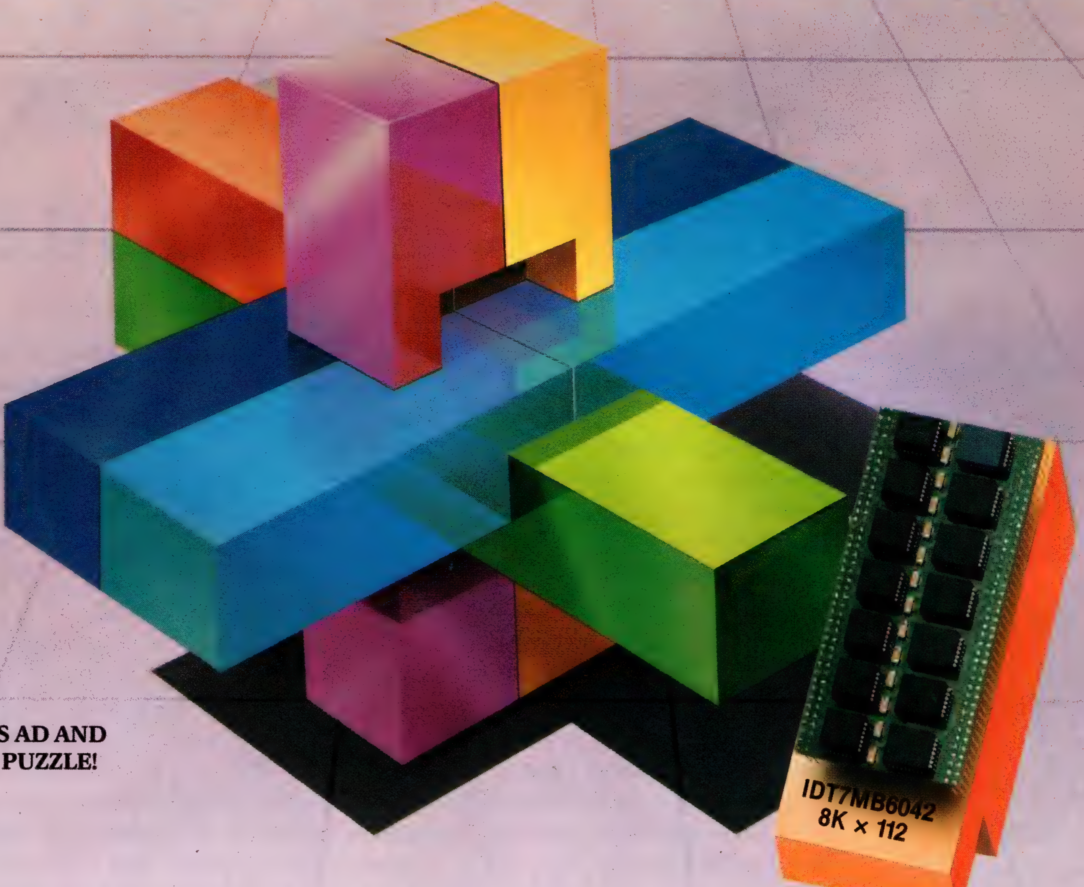

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IR-radiation thermometers

small areas such as semiconductor components, textile fibers, precision-machined parts, and solder joints, independent of the ambient temperature. Therefore, you can control the temperature of these parts with more accuracy.

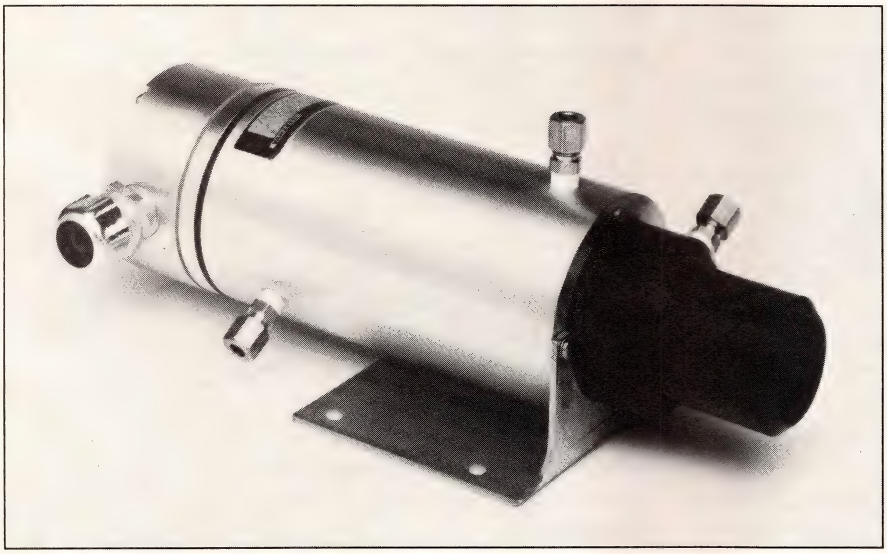
Because an IR-radiation probe doesn't contact the target, the probe maintains a lower temperature than the hot body. Therefore, an IR-radiation thermometer has no upper temperature limit. In contrast, the hot junction of a thermocouple must reach the temperature of the hot body, which places an upper temperature limit on the thermocouple based on the hot junction's melting point.

Certain handheld IR-radiation thermometers are as compact as photoelectric sensors. *The Thermo-Hunter from Capintec Instruments weighs 350g and measures 33×77×77 mm.*

Thermopiles are popular

At the heart of the IR-radiation thermometer is the detector. Most IR-radiation thermometers use a detector with a thermopile, a photovoltaic IR diode, or a photoconductive IR semiconductor. The thermopile is the most popular detector used in IR-radiation thermometers. Athough the thermopile is less sensitive to IR energy than the other detectors, it exhibits a flat spectral response extending from the near IR region (0.7 μm) to the extreme IR region (greater than 50 μm). This feature allows vendors to offer optional IR filters that select wavelength bands to match specific temperature ranges. The other two IR-radiation detectors are more sensitive, but they have spectral responses that peak at wavelengths of less than 10 μm.

A thermopile consists of a large number of thin-film thermocouples connected in series. The junctions of successive thermocouples connect to form a string of sensors. The ends of the string connect to the leads of the detector, which is sealed in a TO-style can. A thermopile doesn't require a bias voltage or current for operation. Because it behaves as a pure resistor, it generates Johnson noise only—no 1/f noise.



The Vanguard II is a 2-wire IR-radiation transmitter with a 4- to 20-mA output signal. *The Vanzetti Systems unit has a 50-msec response time, an accuracy of ±1% of the reading, a repeatability of ±1°C, and operates over 0 to 550°C.*

Dexter Research Center offers a variety of thermopile detectors used in commercial IR-radiation thermometers. The Model 2MC thermopile detector features 36 thermocouple junctions, a sensitivity of 10 volts per watt, a 40-msec thermal time constant, and a resistance of 6 kΩ. The detector costs $38 (100).

EG&G Judson offers a variety of photovoltaic diodes and photoconductive semiconductors for IR-radiation detection. The IR devices, which are made from germanium, indium arsenide, indium antimonide, and mercury cadmium telluride, operate over a wavelength range of 1 to 22 μm. The company also offers the J16Si dual-wavelength detector, which consists of a silicon photodiode mounted with a germanium photodiode in a single TO-style package. The silicon and germanium diodes respond to wavelengths from 0.4 to 1 μm and 1.1 to 1.8 μm, respectively. The device provides two output signals from a single 500-to-1200°C source for use in dual-wavelength temperature sensing. Each device costs $230 to $240, depending on the size of the active area.

Vendors slash their prices

IR-radiation thermometry has progressed on two fronts in the last five years. The first front is cost reduction. In 1985, a typical IR-radiation thermometer with an LCD cost $2500 to $3000. Today, a similar unit costs half that figure. In fact, you can find some units for the OEM market that cost less than $1000.

The devices in Williamson's Transtemp 1000 Series have a base price of $1300 each. Models in the series operate over −40 to +2500°C using thin-film thermocouples that respond to wavelengths from 0.7 to 14.0 μm. The units come in a NEMA-4 enclosure and have an LCD. An operator can adjust the thermal time constant from 0.2 to 5.0 sec and can digitally adjust the emissivity setting from 0.1 to 0.99. (For a detailed explanation about emissivity, see the **box**, "The Importance of emissivity.")

The units operate from a 10 to 40V dc power supply. You supply power to the unit using the same two lines that provide a 4- to 20-mA output signal; hence the unit is known as a 2-wire transmitter. The linear, 4- to 20-mA output signal connects to a recorder or a computer through a current loop. The units also specify an accuracy of 0.75% of full scale and a repeatabil-

The importance of emissivity

All bodies with temperatures above absolute zero (−273°C) possess thermal energy. A certain amount of this energy, which is caused by vibrating molecules, can radiate from the surface of the body in the infrared region of the electromagnetic spectrum. IR-radiation thermometers detect this radiant energy to determine the body's temperature.

For a specified temperature, the maximum amount of radiation a body can emit is called black-body radiation. Black-body radiation is at a known level for every wavelength, and it depends only on the temperature of the emitter. The level of black-body radiation at each wavelength for a specific temperature is given by Planck's Law:

$$W_\lambda = C_1 \lambda^{-5} \left(e^{\left(\frac{C_2}{\lambda T}\right)} - 1 \right)^{-1},$$

where W_λ is the emitter's spectral radiance in W/m^2 for each wavelength; λ is the wavelength in meters; T is the emitter's temperature in degrees Kelvin; C_1 is Planck's first radiation constant, which equals 3.74×10^{0016} W·m^2; and C_2 is Planck's second radiation constant, which equals 1.4388×10^{002} m·°K.

Black-body radiation is only theoretical, however, and it can only be approximated for physical measurement. It exists in the space between the molecules of materials. When the radiation reaches the surface of the material, it's partially reflected, so only a fraction of the radiation emerges from the surface. The fraction emerging from the surface is known as the material's emissivity, a specification that plays an important role in IR-radiation thermometry.

A body's emissivity is the ratio of its emitted radiation to the emitted radiation of a black body at the same temperature. The emissivity is a value from 0 to 1. A gray body has an emissivity less than unity, which is constant for all wavelengths. Three black-body-radiation profiles are shown by the solid curves in **Fig A**. Gray-body radiation is shown dotted for a temperature of 1200°F. The peak of the radiation curves shifts to shorter wavelengths as the temperature increases. In fact, very hot bodies emit energy in the visible spectrum.

A conventional IR-radiation thermometer measures temperature remotely by focusing the radiant energy onto an IR-radiation detector using an optical system. Vendors calibrate the thermometer's temperature indication as if the radiant energy comes from a black body. Because real bodies emit less energy than black bodies, the thermometer must have an emissivity adjustment to calibrate the instruments to the observed radiant energy. The total black-body radiation is given by the Stefan-Boltzmann Law, which is the integral of Planck's Law for wavelengths from 0 to ∞. The Stefan-Boltzmann Law for a gray body that adjusts the thermometer to the target's emissivity is

$$W_{TOTAL} = \epsilon T^4 \sigma,$$

where ε is the emissivity of the gray body; T is the absolute temperature in degrees Kelvin; and σ is the Stefan-Boltzmann constant, which equals 5.63×10^{008} W/m^2/°K^4. The Stefan-Boltzmann Law shows a fourth-power relationship between the total IR radiation and the body's absolute temperature.

Not all materials exhibit gray-body radiation, however. Many materials have strong and weak radiation regions throughout the IR spectrum. Therefore, to match the radiance of a specific material to the IR-radiation detector's sensitivity, IR-radiation thermometers include wavelength-selection filters in the optical system.

The body's emissivity isn't the only factor that ity of 0.5% of the reading value. Options include a water-cooling, air-purging jacket for protecting the lens.

Instruments in the Transtemp 700 Series boast the same specifications as those in the 1000 Series and cost $700 each. Instead of NEMA-4 housing, however, the units have an IR-radiation probe that connects to a circuit board via a cable. Both series have an optional peak detector with an adjustable hold function. The circuit lets you adjust the decay time constant on the peak detector when you're monitoring moving targets with variable emissivities.

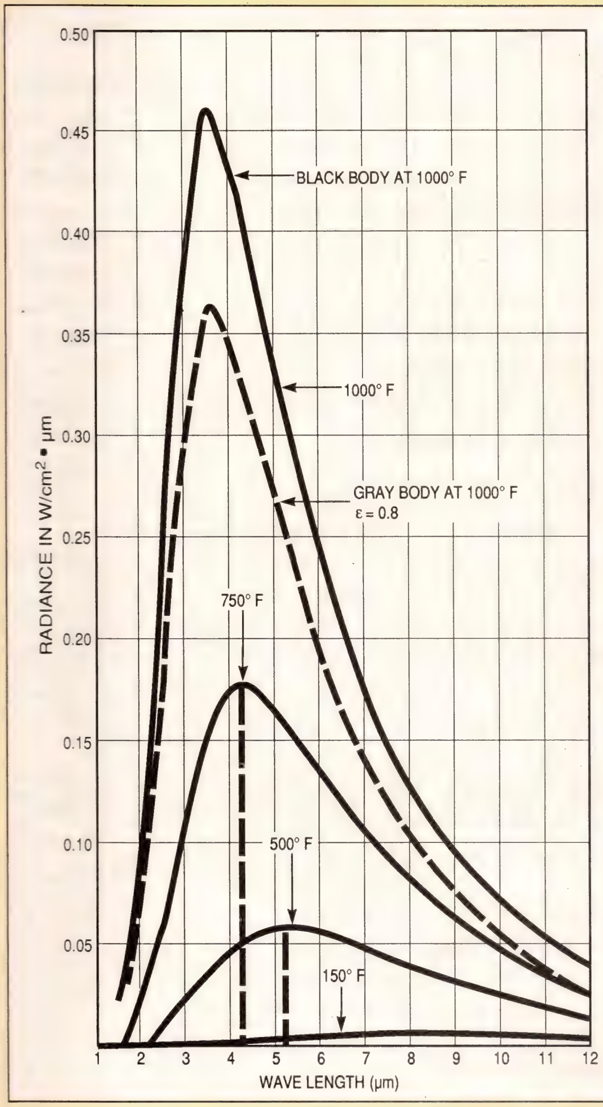
Exergen's Microscanner D-501F IR-radiation thermometer measures temperatures from −50 to +550°C and has a spectral response from 2 to 20 μm. The unit comes in a waterproof housing and specifies an accuracy of ±0.5% of the target temperature for a target with 0.98 emissivity. Repeatability is ±0.25% of the reading value. The thermometer, which costs $649, operates from a 9V alkaline battery.

affects the temperature reading. The optical system must be positioned so that background IR radiation from sources other than the target doesn't enter the system's field of view. In addition, because the optical system doesn't contact the target, IR radiation travels through a medium before reaching the detector. Contaminants in the atmosphere can affect the medium's transmission response and subsequently can decrease the detected IR radiation. To avoid significant errors in the accuracy of the temperature reading, you must calculate an effective emissivity, which compensates for medium-path losses.

Another source of temperature error is the detector's characteristics. Because a body's radiance increases exponentially with temperature, the detector's voltage-vs-temperature curve is nonlinear. Signal-processing circuitry often includes a look-up table that provides a linearized output signal. Thus, deviations from a straight-line curve affect the measurement accuracy.

The IR-radiation detector's ambient temperature can also affect the calibration, particularly when measuring low temperatures (below 200°C). Because the detector is also a hot body, it emits IR radiation, which subtracts from the IR radiation emitted by the target. Therefore, to provide a calibration reference, low-temperature thermometers require an additional temperature transducer to measure the detector's ambient temperature.

The thermometer's ability to compensate for uncertainties determines the absolute accuracy of the temperature reading. However, many applications require repeatability more than absolute accuracy. It's often sufficient if an IR-radiation thermometer produces consistent readings, even though the absolute readings are in error by a few degrees.



Black-body radiation (solid curves) obeys Planck's Law and peaks at smaller wavelengths as the temperature increases. *A gray body (dotted curve) radiates less IR energy than a black body for a given temperature, but it has the same curve shape.*

It has a μP that automatically adjusts the thermometer for the emissivity of the target. The unit provides a linear voltage output that's updated every 100 msec with 0.1° resolution. It also contains a peak detector with a hold function and an audible alarm indicator for monitoring maximum and minimum temperature readings.

Capintec Instruments' ThermoHunter Built-in Series also costs less than $1000, with prices starting at $900. Models in this series operate over −50 to +1000°C. The units use either thin-film thermocouples or lead-selenium photodiodes as detectors, which have thermal time constants of 500 and 80 msec, respectively. Because the lead-selenium detectors operate in the 1- to 4-μm range, they can measure temperature through glass. A delay function allows the units to measure the mean temperature in an adjustable time frame of 0 to 7 sec. The units provide a linear-voltage-output signal.

Fiber optics boosts sensing

In addition to their reduced prices, IR-radiation thermometers are also more sophisticated than their predecessors of five years ago. These devices now offer fiber-optic wave guides, single-lens reflex focusing, portability, advanced signal processing, and dual-wavelength sensing—features that previously weren't economically feasible.

By assembling quartz optical fibers into fiber bundles, optical wave guides can transmit energy in the near infrared region—a region that was once opaque to IR energy. The optical cables are flexible, so IR-radiation thermometers equipped with fiber-optic cables can look around obstacles to measure temperatures from 300 to 2000°C. The IR fiber-optic cables connect to an optical system located at the viewing end of the cable. The wave guide transmits the energy to a detector and amplifier remotely located from the heated surface.

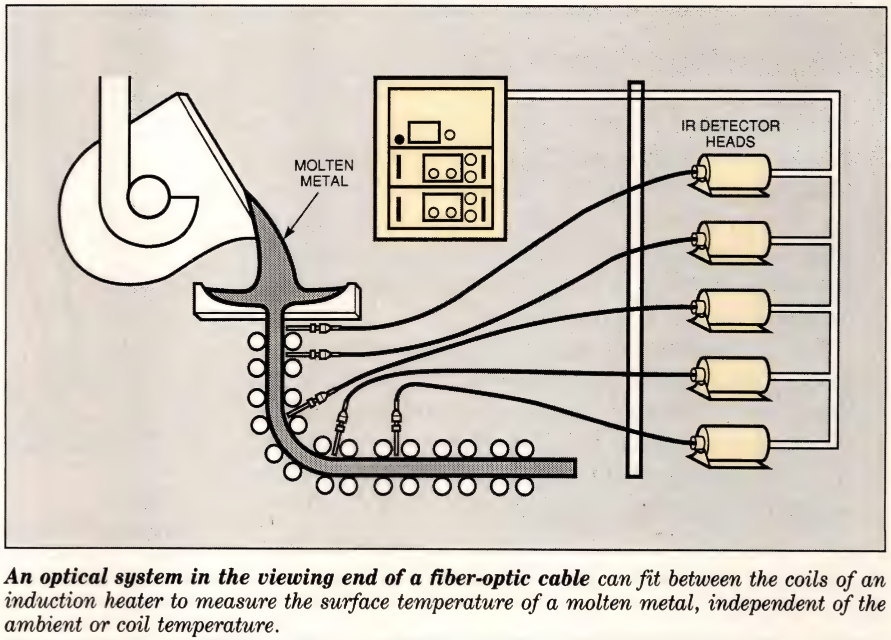
Portability and a built-in μP that performs automatic emissivity compensation *are two features of Exergen's D-501F IR scanner. The unit operates from a single 9V battery and updates the output signal 10 times/sec.*

Applications for fiber-optic temperature sensing abound. For example, fiber-optic sensing lets you obtain a much more precise temperature measurement of a molten metal heated by induction coils. You can place the viewing end of the cable between the coils, permitting the thermometer to measure the molten-metal temperature independent of the coil temperature (**Fig 1**).

Vanzetti's LTD Series linearized IR-radiation detector/amplifiers are designed for use with flexible fiber-optic cable. Specifications include an accuracy of ±1% of the reading, a repeatability of ±0.1% of the set-point, and a thermal response time from 100 to 5 msec. The device chops the IR energy at a 400-Hz rate, permitting synchronous demodulation to discriminate against electromagnetic noise at other frequencies. The LTD 4035-S operates over a wavelength range of 0.8 to 1.05 μm and costs $1755.

The Land Fiberoptic is another series of IR-radiation detector/amplifiers designed for use with flexible fiber-optic cables. Units use either a silicon or a germanium detector cell. The FP11 model has a silicon cell that responds to wavelengths from 0.7 to 1.0 μm. The model specifies an accuracy of ±0.25% of the absolute temperature in °K+2°C, a repeatability of ±0.15% of the absolute temperature in degrees Kelvin, and a thermal time constant of 5 msec. Prices range from $1600 to $2000.

Advances in CMOS technology have made handheld noncontact thermometers a reality. Raytek and



An optical system in the viewing end of a fiber-optic cable *can fit between the coils of an induction heater to measure the surface temperature of a molten metal, independent of the ambient or coil temperature.*

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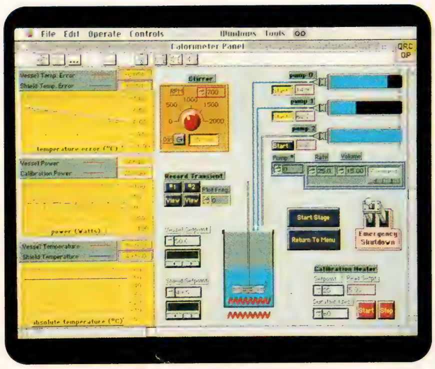
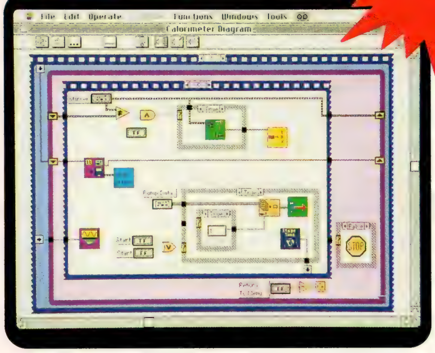


LabVIEW 2 front panel user interface



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Ircon are only a few of the companies that offer standard handheld products that operate from batteries. Ircon's Ultimax is a handheld unit that contains a number of user-friendly features. It operates in a similar manner to a single-lens reflex camera. The thermometer contains a dichroic mirror that transmits visible energy and reflects IR energy, so you can view an object through the mirror while the IR energy from the object reflects off the mirror to an IR-radiation detector.

The Ultimax contains a µP for signal processing; this chip responds to pushbutton controls for setting the emissivity, thermal response time, and peak-detector decay time. Models operate over −50 to +3000°C, covering six different IR regions. Response time ranges from 0.5 to 2.0 sec depending on the model, and the repeatability is within 1.0°C of the reading. In addition to providing an LCD, the thermometer has a linearized 0-to-1V analog output and an RS-232C port for sending logged data to a computer or printer. The unit, which costs $2250, weighs 1.9 lbs and uses four AA alkaline batteries that operate for 20 continuous hours.

Two colors cancel emissivity

All of the IR-radiation thermometers discussed so far are single-wavelength devices that determine temperature by measuring the brightness of a target. If the target has a low emissivity, the instrument will provide a low temperature reading because the brightness is low. Therefore, to ensure accurate readings, single-wavelength thermometers must have an emissivity adjustment.

In contrast, dual-wavelength (2-color) thermometers, which appeared less than five years ago, are insensitive to emissivity. Therefore, they can provide accurate temperature readings in the presense of dust, steam, smoke, and other particles in the air. These thermometers take the ratio of the responses to two different IR wavelengths. If a target's emissivity is the same for both wavelengths (a good assumption when the wavelength bands are adjacent), the emissivity effect cancels. The output of the dual-wavelength thermometer at high temperatures is approximately

$$E_0=\frac{W_{\lambda 1}}{W_{\lambda 2}}=\left(\frac{\lambda_2}{\lambda_1}\right)^5 e^{\left[-C_2\left(\frac{\lambda_2-\lambda_1}{\lambda_1\times\lambda_2}\right)\frac{1}{T}\right]}.$$

Furthermore, dual-wavelength thermometers are insensitive to any changes in the target's field of view. If an obstruction or the target's orientation result in a low brightness reading, the effect occurs at both wavelengths; therefore, they both cancel when the radiometer takes the ratio of the two readings.

Both Land Instruments' System 3 Series and Williamson's Tempmatic 8000 Series contain thermometers based on the dual-wavelength principle. The thermometers have a front-end, motor-driven cylinder that has mounts for two selective IR filters. The control circuitry synchronizes the motor's position so that a single detector can alter-

For more information . . .

For more information on the IR-radiation thermometry products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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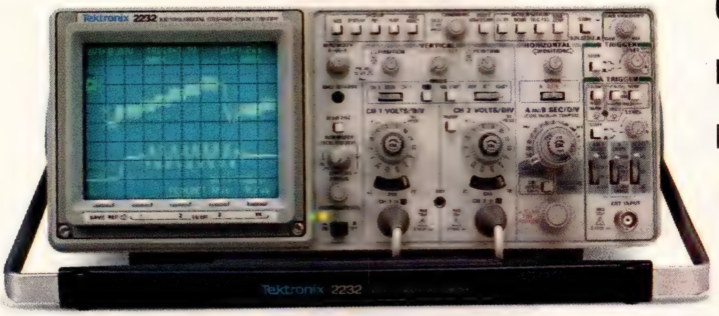

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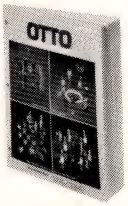

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IR-radiation thermometers

nately receive IR energy in the two bands. The succeeding circuitry takes the ratio of the two readings. Certain models in the Tempmatic Series operate over a temperature range of 150 to 2400°C. Units in the Tempmatic Series start at $2600, which includes the dual-wavelength processor and a visual-aiming feature. Land Instruments' Ratio Thermometers operate over 250 to 4200°C and cost $5000 each, including the dual-wavelength processor.

To help you gain a more thorough understanding of the complexities of IR-radiation thermometry, manufacturers provide technical support and numerous application notes for their products. In addition, they offer a variety of accessories, including black-body radiation calibrators; NEMA-qualified housings; air-purging and -cooling jackets; optional, thermocouple-compatible output ports; PID (proportional-integral-derivative) controltlers; power supplies; meters; fiber-optic cable; and an assortment of optical systems. **EDN**

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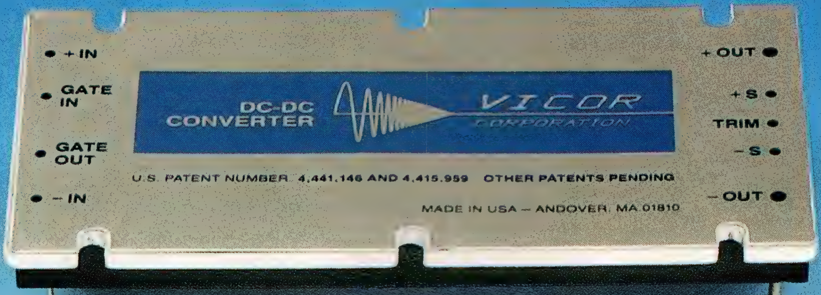
EDN Magazine's March 1, 1990, issue will feature a staff-written Special Report on Macintosh-based CAE/CAD software and the final installment of the designer's guide to Spice-compatible op-amp macromodels. Another feature story will describe how to build testable ASICs using nonstructured design techniques.

Remember to look for our regular departments, too.

1985 : smallest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CIRCLE NO. 80

Fiber-optic connectors come of age

Today's high-performance optical connectors satisfy the needs of the most exacting commercial, industrial, and military applications.

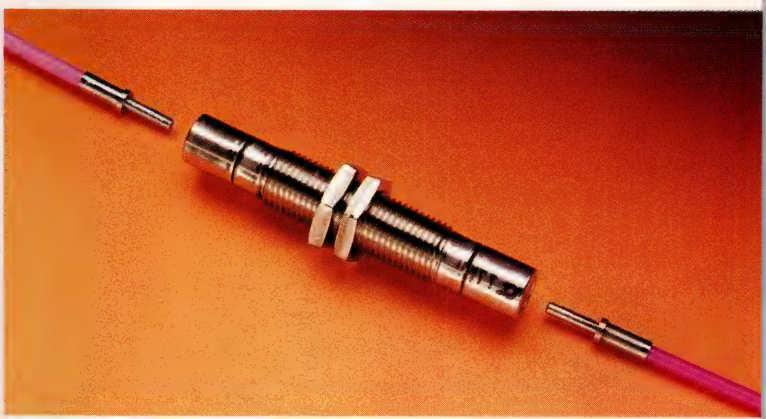
Tom Ormond,
Senior Editor

Connectors play a vital role in fiber-optic system performance. The components couple fibers to sources, detectors, and other fibers throughout a communications system, and they accomplish these tasks both reliably and economically. To find out which fiber-optic connector is best suited to your application, you must consider a number of factors, such as insertion loss, termination requirements, and bottom-line cost.

When you're evaluating a fiber-optic connector, one of your most important concerns is that the device must introduce minimal optical-power loss across the interface. In addition, the loss characteristics of the connector must be consistent and should exhibit little change over numerous connect/disconnect cycles. Further, the connector should be easy to install without special tools or special training. Finally, the installed cost, or bottom-line cost, of the connector must be inexpensive when you consider both the initial cost and the cost of termination.

You can choose from an ample selection of connectors. As you can see in **Table 1**, you'll have little trouble finding a device with loss figures below 0.5 dB. In addition, every device listed in the **table** is field installable. Certain connectors require the use of epoxy adhesive in the termination process, but many connectors have a dry-termination capability. Adhesives do increase termination time, and extra time means extra costs. Of course, the length of your transmission determines how critical the cost factors are. For example, if your application requires six connectors to transmit information over 30 km, then a bottom-line cost of $50/device isn't unreasonable. On the other hand, if your application has transmission distances of hundreds of meters, using $50 connectors would be too expensive to be a viable choice.

Precise alignment is the key to improved connector performance. Basically, there are two types of fiber-to-fiber interconnection: butt coupling and lensed beam. In the former technique, you position the two fibers in high-precision ferrules and polish them to develop an extremely fine face finish. Then, within a common alignment sleeve, you bring the fibers into actual contact or as close together as possible to minimize



***Designed for single-channel, fiber-to-fiber applications,** ITT Cannon's In-Line Cable Adapter accepts MIL-T-29504/4 optical pin contacts. The unit features a retention clip and a cable-sealing grommet that retain the terminus and ease pin installation and removal using standard tools.*

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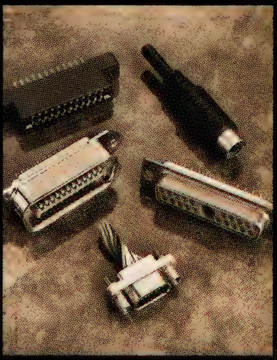

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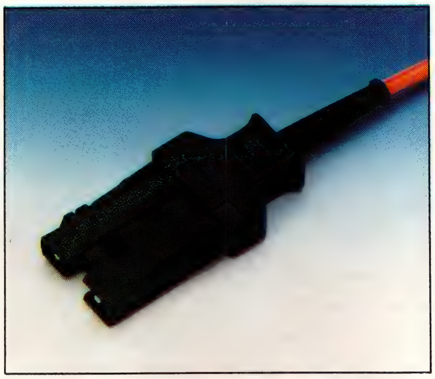
CIRCLE NO. 81

insertion loss. In the latter technique, expanded-beam interconnections introduce a lens system between the two fibers. The light emerging from one fiber is captured and collimated by the first lens and projected across the gap to the second lens. The second lens receives the light and refocuses it onto the receiving fiber. First we'll look at the techniques employed in butt-coupled connectors.



Aimed at cost-sensitive commercial applications, *Siemen's FDDI MIC duplex connector provides the maximum possible packing density while still allowing handling comfort.*

ST-type connectors are popular

The ST-type connector, which was developed by AT&T, is the predominant choice for moderate-distance applications. Many manufacturers offer these devices. Augat's SMT Series connector system features a keyed, bayonet-latching coupling mechanism to guarantee consistent alignment with every connection. The devices are designed to accommodate any multimode application and are fully compatible with other ST-style fiber-optic connectors.

The SMT connector is made of nickel-plated zinc and is available with either a ceramic or metal ferrule. A proprietary machining operation ensures that the metal ferrules will feature tight tolerances and long-term durability. Standard connector sizes accommodate fibers with 125- or 140-μm cladding diameters; an in-house precision drilling capability allows the company to customize the SMT connector to accept other fiber sizes.

Augat offers a complete SMT connector system. You can terminate the connectors in the field or purchase the connectors from the factory, preassembled as part of a cable assembly. In addition, you can order panel-mountable interconnects, active-device receptacles, and a complete, easy-to-use field-termination kit.

Augat isn't the only manufacturer offering its own version of the ST connector. In fact, certain vendors have taken a new approach in the design of these devices. The Pre-Cap Series from Thomas & Betts consists of a complete line of common fiber-optic-connector designs that include SMA, ST, and FC types. The units, which combine the rugged construction of a thermotropic, liquid-crystal polymer alloy with the precision tolerance of a glass capillary, provide both performance and durability in applications that involve multimode glass fibers.

A precision-manufactured (1-μm tolerance), 10-mm-long glass capillary that matches the thermal stability of the glass fiber helps the Pre-Cap connector achieve high performance. The units are compatible with simplified crimp-and-polish termination techniques and can accommodate fibers with 125- or 140-μm fibers.

The polishable connectors provide a reduced contact area that increases connector performance. Also, because the fiber and capil-

Table 1—Representative fiber-optic connectors

Manufacturer	Model	Fiber type	Fiber capacity	Field installable	Ferrule material	Fiber size (μm) (core/OD or OD only)	Insertion loss (dB)	Price
AMP	FSD	multimode	2	yes	ceramic, steel	125, 140	0.6	$16 to $25
Amphenol	944 Series	single mode	1	yes	ceramic	9/125	0.35	$15 (100)
AT&T	ST II	multimode	1	yes	ceramic	125	0.6	$6 to $12[1]
Augat	SMT	multimode	1	yes	ceramic, steel	125, 140	0.6 max	$10[2]
ITT Cannon	FOCT	multimode	1	yes	ceramic	125, 140	0.5	$12 (100)
Lemo	FFS	multimode	1	yes	steel	125	1.5	$93/mated pair
Methode	908/MST	single mode, multimode	1	yes	ceramic	8.3 to 100	0.5 (SM), 0.5 (MM)	$8.70 (1000)[3]
Siecor	Field-installable ST-compatible	multimode	1	yes	ceramic	125	0.2	$10
Siemens	FDDI MIC	multimode	2	yes	zirconia	62.5/125	0.5	$180[4]
Thomas & Betts	Pre-Cap	multimode	1	yes	polymer	125, 140	0.3	$7.95 (1000) for SMA & ST types

1. Per kit, which contains crimping sleeve, cable support boot, and assembled connector
2. Ceramic ferrule version
3. Multmode versions
4. For an assembly with two connectors and a 5m cable

lary are polished as one glass surface, the polished connector provides a smooth, flat, nonconcave fiber end surface. This technique allows installers to eliminate fiber-surface imperfections while employing automatic polishing equipment to reduce termination time.

The connector designs discussed so far have been aimed at applications involving multimode fibers. However, certain manufacturers are concentrating on developing connectors for single-mode fiber applications.

The increasing complexity of single-mode fiber-optic systems has put more emphasis on precision-alignment techniques to keep insertion loss low. The faster transmission speeds and the heightened sensitivity of single-mode systems intensify the need to select the proper connector for the job. To satisfy the demands of modern single-mode systems, the connector must have low insertion and return losses, high mechanical stability and repeatability, and it must be easy to terminate.

The tighter tolerances that manufacturers can achieve with today's ferrule materials help minimize the insertion loss in most modern connectors. AMP enhances this performance by using a termination technique called physical contact. This technique provides a radiused polished surface that allows the two fibers at an interface to optically touch. This optical contact—less than a quarter of the transmission light's wavelength separates the fibers—markedly reduces Fresnel loss (see **box**, "Facts about interconnect loss"). In many cases, Fresnel loss can be as high as 0.3 to 0.4 dB at any interconnection.

In addition to reducing insertion loss, the physical-contact technique offers single-mode fiber systems a

Facts about interconnect loss

When you connect two fibers, the misalignment of any center axes will lead to interconnect losses. Three factors contribute to the loss specification in a fiber-optic interconnection: intrinsic factors related to fiber variations, extrinsic factors that are a function of the connector design, and system-related factors. This discussion will concentrate on extrinsic factors. The main extrinsic problems that cause interconnect losses are lateral displacement, end separation, angular misalignment, and surface roughness.

Lateral displacement occurs when a connector fails to accurately align the center axes of the two fibers, resulting in loss. The amount of loss is a function of the ratio of the lateral offset to the fiber diameter, so the acceptable offset value decreases as the fiber diameter decreases. A 10% core-axis displacement will develop a 0.5-dB loss. Obviously, lateral displacement becomes more critical as core diameter decreases.

The end separation of two fibers causes two types of losses. Fresnel reflection loss results from the difference in the refractive indices of the two fibers and the gap between the fibers, which is usually air. Fresnel losses occur at both the source and receive fiber face. To reduce Fresnel losses, certain manufacturers use index-matching fluids between the two fibers. This optically transparent fluid has a refractive index that matches that of the fibers.

The second end-separation-related loss occurs in multimode fibers. Light exiting a fiber spreads out conically as a function of the fiber's numerical aperture. If the source fiber has a larger numerical aperture, the high-order modes of light will miss the acceptance cone of the second fiber at the other side of the gap. The goal is to minimize end separation, so the ideal situation would be a zero gap (the fibers actually touch). However, this condition could mar the fiber surfaces during the interconnect procedure.

Another problem that contributes to loss is angular misalignment. Optimally, the ends of the mating fibers should be perpendicular to the fiber axes and to each other. When one fiber face is misaligned, losses occur, and the degree of these losses depends on the numerical aperture of the two fibers. In this case, however, a larger numerical aperture can tolerate a larger angular misalignment. Today's connector designs can control angular misalignment, so this loss doesn't contribute as much as lateral displacement does to overall connector losses.

Surface finish is the final factor that contributes to interconnect loss. The surface finish is more of a termination problem than a connector-design problem. As long as the connector's design maintains a substantial gap between the fibers and ensures that no degrading facial abrasion occurs during the mating process, a smooth surface finish depends on the ability of the connector installer. The installer must ensure that the fiber faces are smooth and defect free. Any defects will disrupt the light-ray transmission pattern and increase interconnection losses significantly.

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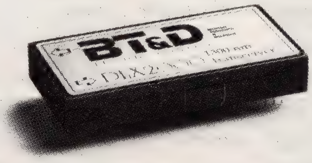

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second advantage that's just as critical: It minimizes return loss, which is a function of the interface reflections. It's particularly important that you minimize these return losses in analog-transmissions systems, where they can cause the most damage. Single-mode transmitters use laser diodes as their light source. Lasers amplify light, so if the interface reflections have sufficient magnitude and occur at the proper wavelength, the laser will amplify them.

According to connector designers at AMP, a typical noncontacting interconnection will exhibit about 15 dB of return loss. A factory-prepared, physical-contact interface typically exhibits a return loss of more than 40 dB, significantly reducing reflection effects on a transmitter.

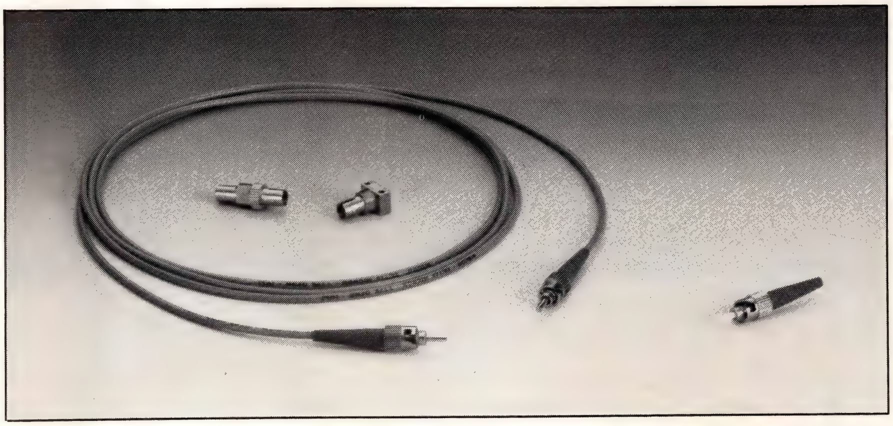
Today's fiber-optic connectors are reliable enough to handle military applications. ITT Cannon manufactures the In-Line Cable Adapter and Device Receptacle connectors, both of which are designed for use in avionic fiber-optic links. The Device Receptacle, which includes a mounting mechanism, is designed to save weight and simplify fiber-to-device coupling. This design offers users an alternative to the industry-standard practice, which houses the active device in an SMA receptacle connector, which is then mated to an SMA plug connector. To align the fiber to the device, a coupling nut joins the receptacle to the plug.

The Device Receptacle accepts a MIL-T-29504/4 pin contact and costs $57 (100). It contains a retention clip and a cable-sealing grommet that retain the terminus and simplify contact installation and removal with the use of industry-standard, size-16-contact insertion/extraction tools. This scheme eliminates the need to employ multiple contact types throughout the fiber-optic link, and it lets you use the same tools throughout the system.

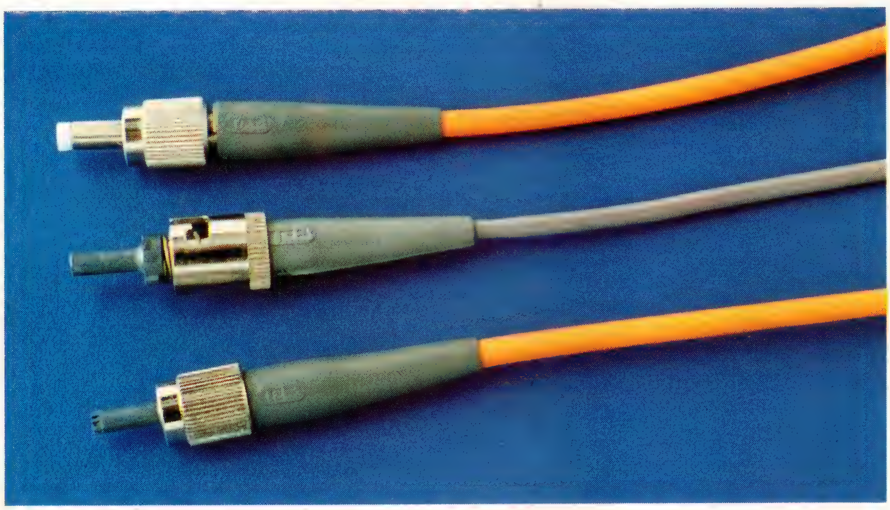
The In-Line Cable Adapter is designed for single-channel, fiber-to-fiber applications. It accepts ITT Cannon's MIL-T-29504/4 optical pin contacts, and it can be used individually or with the company's MIL-C-38999 connectors and Device Receptacle in a fiber-optic link. Again, this connector allows you to use the same tools throughout the system.

The adapter is lightweight and compact, and it contains the same retention-clip mechanism used in the MIL-C-38999 connector and Device Receptacle. It also features a cable-sealing grommet and is designed to allow users to use a standard insertion/extraction tool to install and remove the contacts. The In-Line Cable Adapter costs $84 (100). The Defense Electronics Supply Center (DESC) is in the process of drafting MIL-spec slash sheets for the In-Line Cable Adapter and for the pc-board and flange-mount versions of the Device Receptacle.

The other method of fiber-to-fiber interconnection, in addition to the



Available with either a ceramic or steel ferrule, *Augat's SMT connectors feature a keyed, bayonet-latching mechanism. They're designed for multimode applications and are fully compatible with other ST-style connectors.*



Compatible with all styles of optical cable *available from major manufacturers, Pre-Cap Series connectors from Thomas & Betts employ a polymer alloy combined with a glass capillary to provide 0.3-dB max insertion loss. They accommodate 125- and 140-µm multimode fibers, and a crimp-and-polish procedure enables you to readily terminate them in the field.*

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One good idea after another.

CIRCLE NO. 83

butt-coupled technique, is the lensed-beam technique. Cinch Connectors is developing lensed crimp-and-cleave termini for MIL-C-26500 and MIL-C-38999 connectors using both gradient-index rod lenses and precision ball lenses. To understand the company's lensed design, you must be familiar with the present form of the MIL-C-26500 terminus.

The beam expansion and collimation is performed by a 1-mm Selfoc lens in the front of each contact. A distance of 0.006 to 0.008 in. separates the fiber from the lens. Because the surfaces never touch, it's unlikely that the cleaved fiber or the lens will be damaged during termination or subsequent environmental or mechanical stress. The use of rod lenses means that the fiber end face is flat—a feature that facilitates field cleaning. Finally, the lenses have antireflection coatings to minimize loss due to back reflection.

A precision fiber guide laterally aligns each fiber with its lens. This guide is typically made of sapphire or ceramic. Behind the fiber guide is an alignment sleeve. This sleeve serves two purposes: It mechanically holds the fiber guide in position, and it steers the entering fiber into the fiber guide.

A coupling sleeve that brings the pin and socket into close alignment is attached permanently to the socket terminus. The sleeve's dimensions and hardness, combined with the close tolerances on its inside diameter and on the outside diameter of the pin terminus, ensure that only extremely high values of pin/socket torque could twist the two out of close angular alignment.

A crimp sleeve, the final connector part, strengthens the termination. This sleeve, which accommodates Kevlar or fiber-glass strands, captures the material between two metal layers to maximize crimp strength. With a termination time of well under five minutes, the terminus offers a potentially cost-effective choice for high-performance, fiber-optic cable assemblies that use military cylindrical connectors.

Article Interest Quotient
(Circle One)
High 518 Medium 519 Low 520

For more information . . .

For more information on the fiber-optic-connector products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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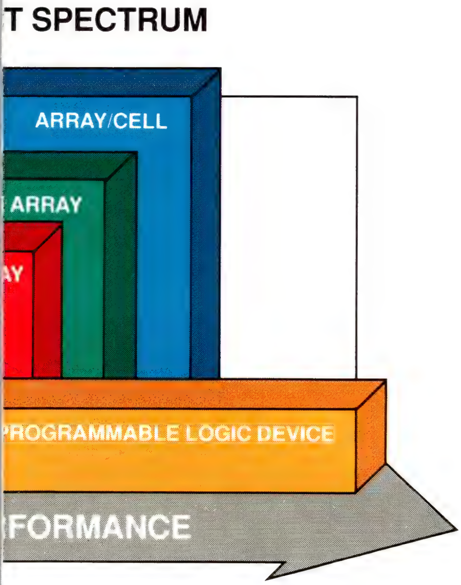
For details about the support and service TI offers, please turn the page.



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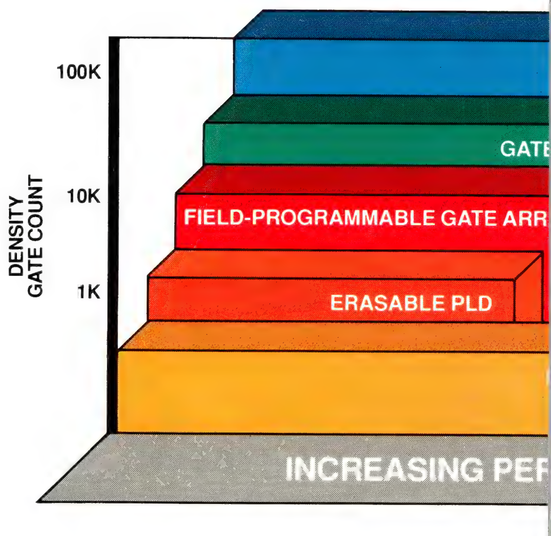
TI's ASIC PRODUC



A PERSPECTIVE ON ASIC DESIGN

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Wally Rhines

Walden C. Rhines, Ph.D.
Executive Vice President, Semiconductor Group
Texas Instruments Incorporated

IN THE ERA OF MEGACHIP TECHNOLOGIES

On my schedule,
ivery delays and
necessary risks are
. Our design
uires the density of
ate array, but we
d to handle all the
grammation
rselves. ”

TI Solution:

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Gate Arrays

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The TI Solution:

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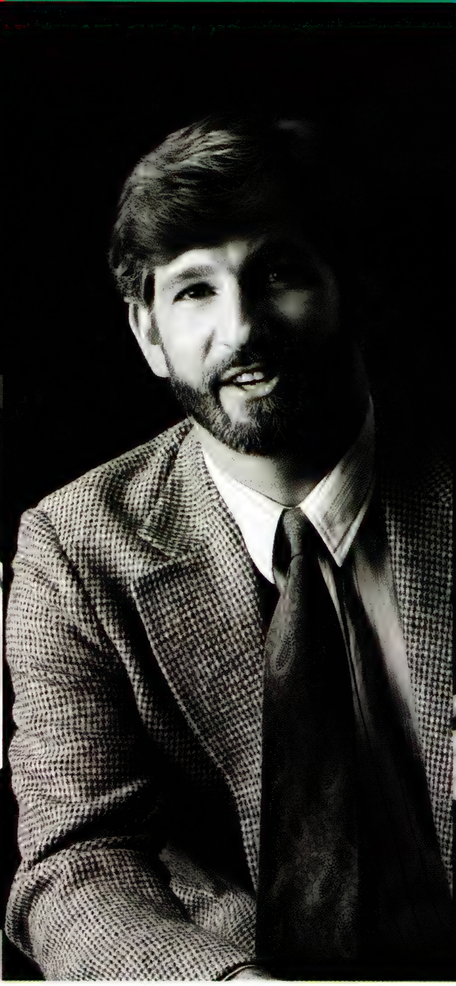

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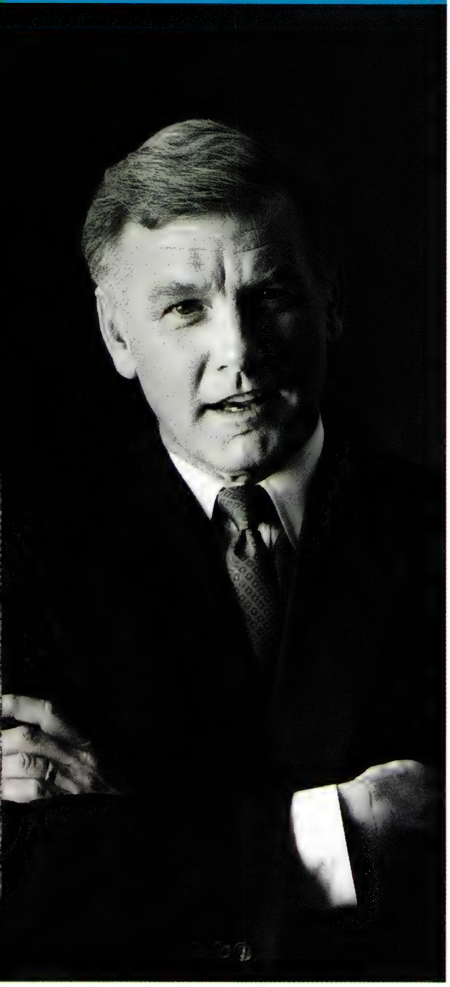
The TI Solution:

Standard Cells



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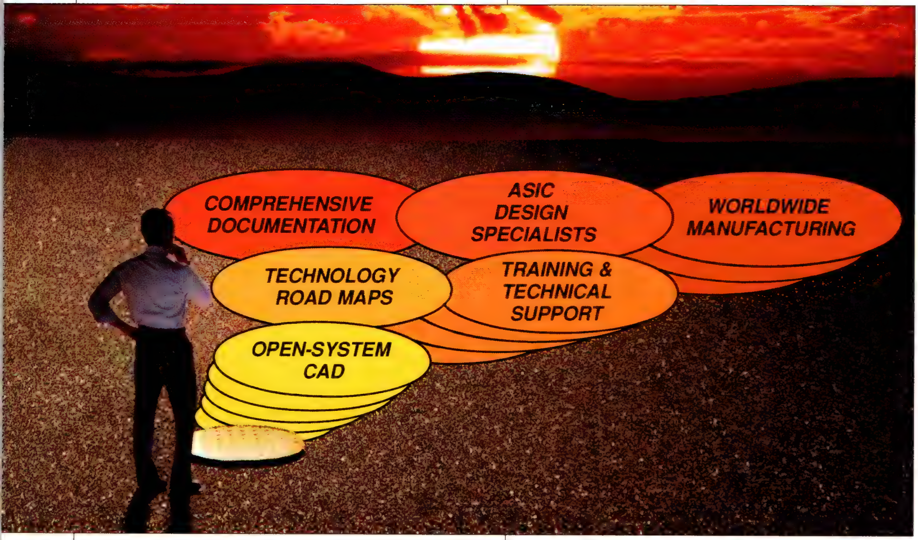
Our design flow is straightforward and minimizes the possibility of surprises.



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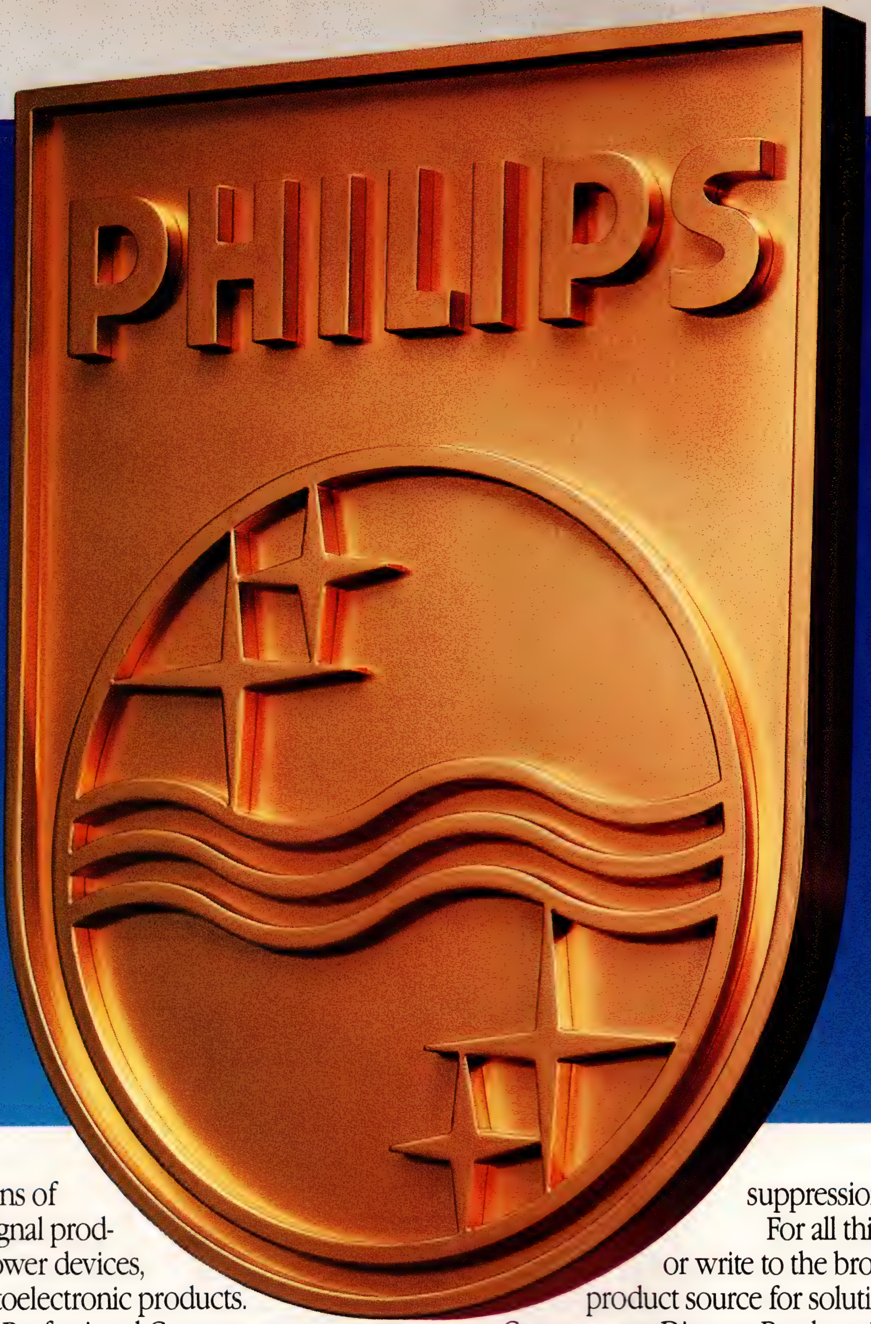

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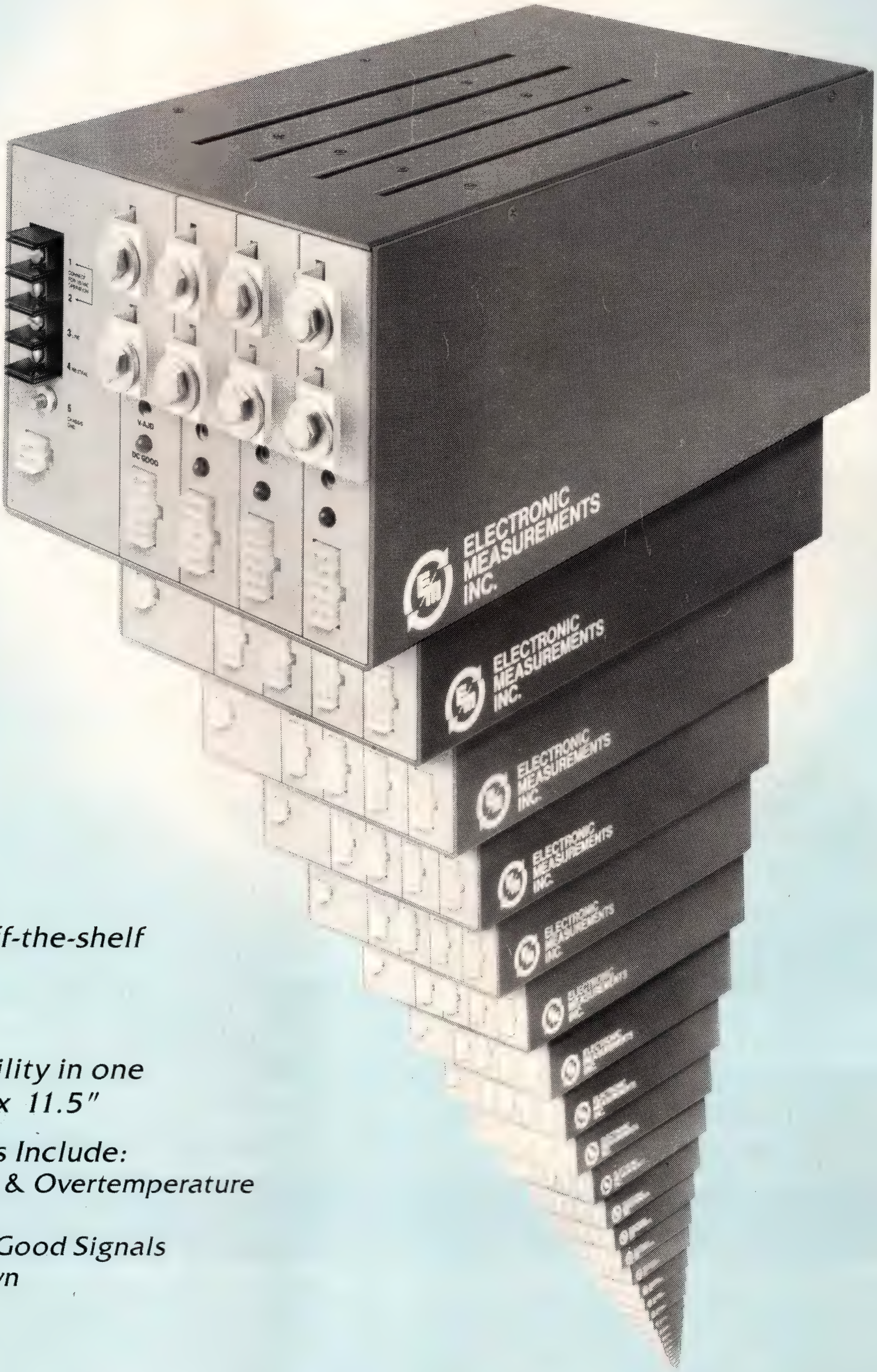

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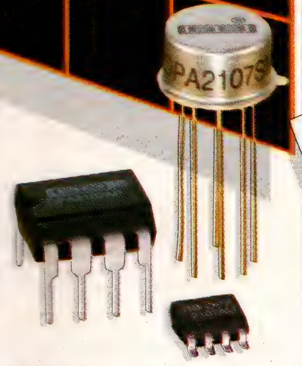

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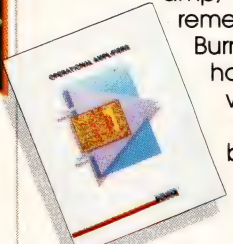

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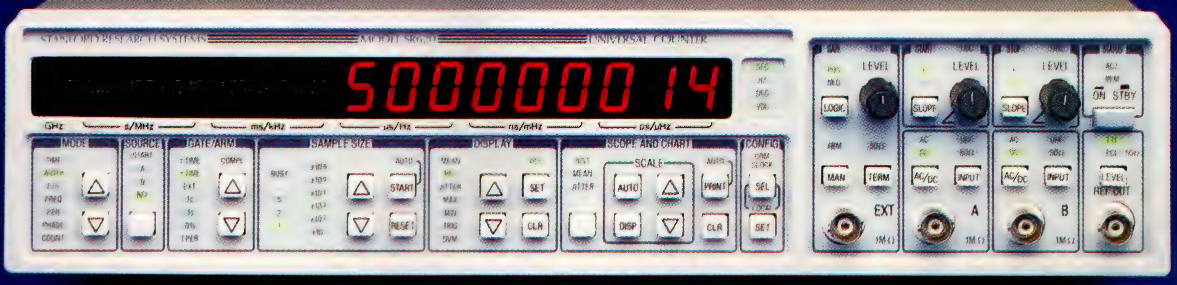

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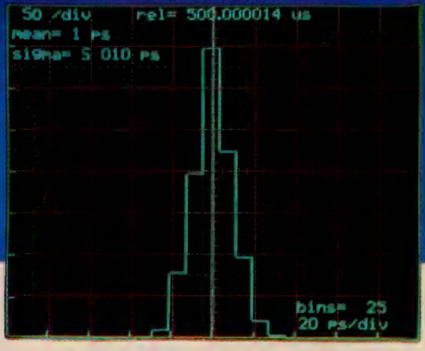

The SR620 provides graphic display of histograms and strip charts on any X-Y oscilloscope. With Autoscale and Zoom, graphics can be easily scaled. Attach a dot matrix printer or an HP-GL plotter and obtain hardcopy of any graph.

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GRAPHICS LIBRARIES FOR PCs

Graphics libraries ease your development task

If you need graphics in the applications you develop, don't reinvent the wheel. There exist many graphics libraries that can simplify your task—especially if your programs will run under MS-DOS Windows or OS/2 Presentation Manager.

Chris Terry,
Associate Editor

The requirements of the applications you are developing determine the need to incorporate extensive graphical capabilities for the user's benefit. If you're designing CAD/CAM or CAE systems, the point is almost moot—these systems handle material that is primarily graphic and so need all the graphical capabilities of the workstation on which they will run. But designing a business system is a whole different ball game.

Many of the big vendors, such as IBM, Microsoft, Sun Microsystems, and Apollo, would have you believe two things: that a graphical user interface (GUI) is already a necessity for any new application; and that in two or three years a program that doesn't have a GUI will be totally unacceptable to all end users. If you believe either one, you might consider putting in a bid on the Brooklyn Bridge, for resale to Japan.

A huge number of applications (including word processors, database search-and-retrieval systems, accounting systems, management-information systems, and data-acquisition or instrumentation systems that build and execute command files) still handle primarily characters (letters and numbers). These applications don't need a full-blown GUI. They may, however, benefit from a windowing system that provides users with explicit menus to guide them to the function they need, and from on-line help screens to clarify complex procedures. But the windows that help these users are relatively simple and are a far cry from the complexity of MS Windows—and even further from that of OS/2's Presentation Manager. Also, in character-based systems, a mouse is often a hindrance rather than a help.

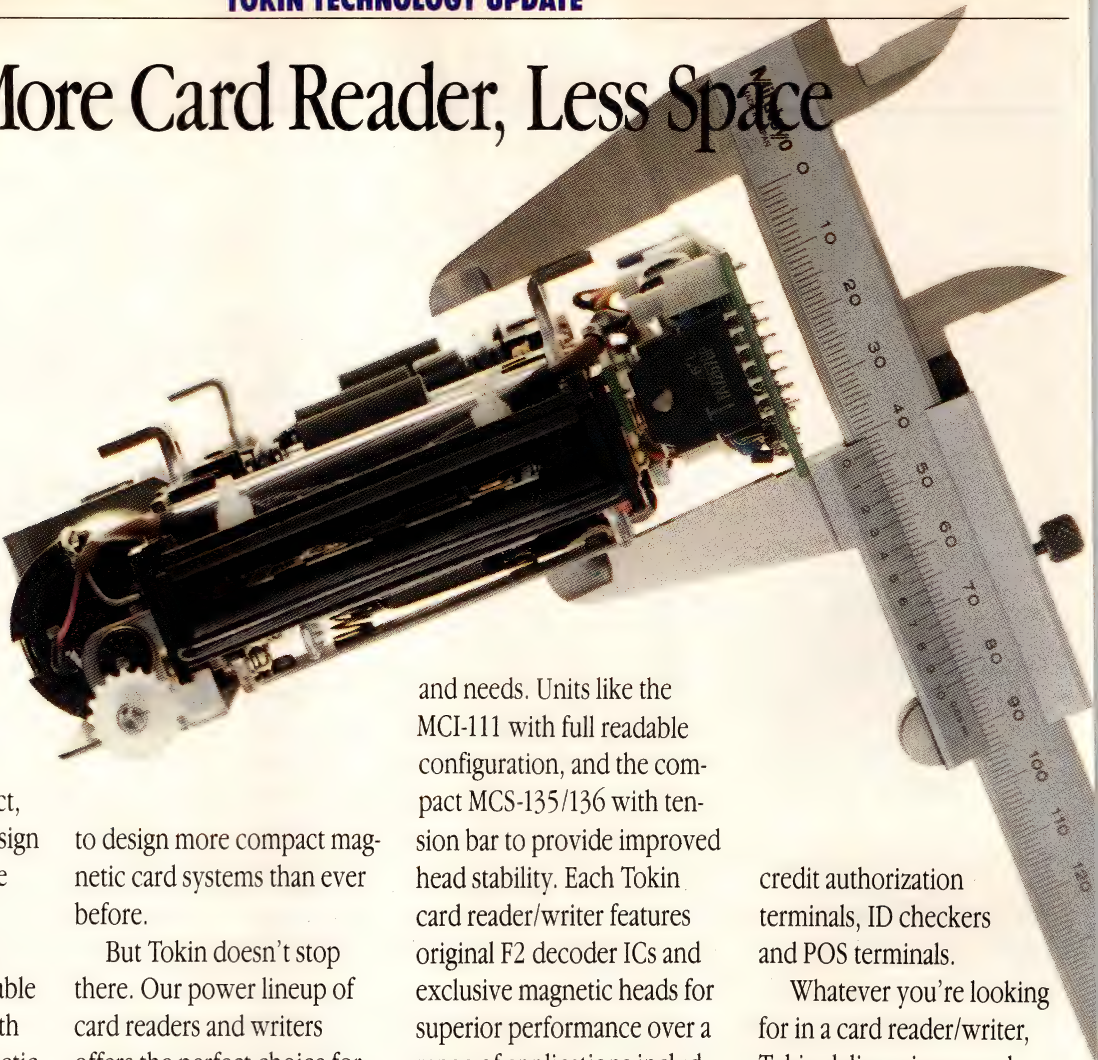
Bruce Tonkin (**Ref 1**), a programming consultant in the Chicago area, points out that the main source of user resistance to GUIs is money, rather than innate conservatism. In the Midwest, he finds, most PC users are small or mid-sized companies that have 20 to 50 computers, of which perhaps half are IBM PC/XTs or XT clones, the other half being 80286-based machines, all with Hercules-compatible boards and monochrome displays.

To install and effectively use Windows or Presentation Manager, a company would need much more expensive 80386-

A graphics tool kit lets you create complex images *without needing to write low-level routines. (Photo courtesy GSS)*

TOKIN TECHNOLOGY UPDATE

More Card Reader, Less Space



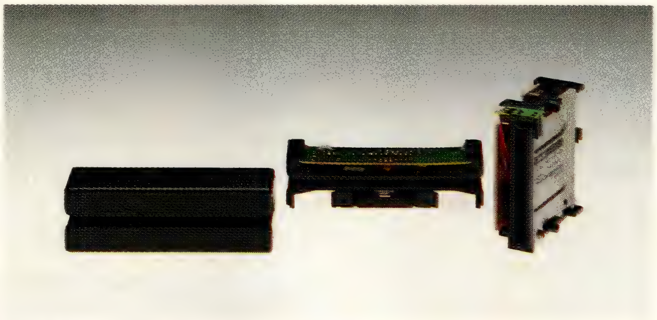
It's here. The designer's dream. A motorized card reader so small, so compact, so lightweight, you can design it into any system you dare imagine.

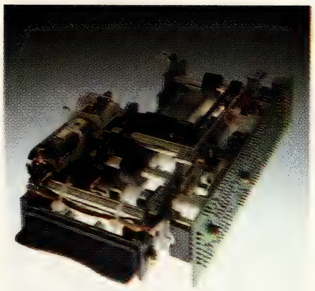
Tokin's new MCA-1601 boasts the kind of impeccable design that only Tokin, with a full half-century of magnetic engineering achievements, can produce.

The MCA-1601 overcomes card readers' biggest drawback—size. Slim (46mm) and lightweight (700 g), it gives you the power and flexibility to design more compact magnetic card systems than ever before.

But Tokin doesn't stop there. Our power lineup of card readers and writers offers the perfect choice for a vast range of specifications and needs. Units like the MCI-111 with full readable configuration, and the compact MCS-135/136 with tension bar to provide improved head stability. Each Tokin card reader/writer features original F2 decoder ICs and exclusive magnetic heads for superior performance over a range of applications including strip card readers for credit authorization terminals, ID checkers and POS terminals.

Whatever you're looking for in a card reader/writer, Tokin delivers improved performance and flexibility, and the opportunity to design card systems that match your most demanding specifications. Check us out.





Manual magnetic card reader/writer unit

Model	Card standard	Features	Dimensions (mm)
MCS-135	ISO 3554 Track 1 and 2	One way, double track: simultaneous reading	100×32×32.5 (with cover)
MCS-136	ISO 3554 Track 2 and 3	One way, double track: simultaneous reading	
MCI-111	ISO 3554 Track 2	Magnetic card insertion system	67×65×24

Motorized magnetic card reader/writer unit

Model	Card standard	Features	Dimensions D×W×H (mm)
MCA-1601	Accepts all standards	Extremely thin and half the volume*	183×139×45.4

*Compared with conventional Tokin models.

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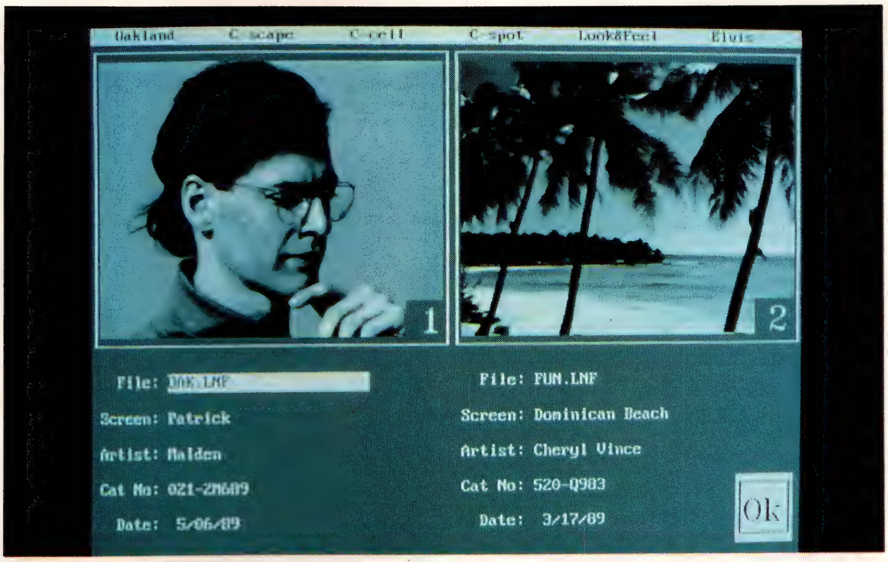


File: OAK.LNF
Screen: Patrick
Artist: Malden
Cat No: 021-2M689
Date: 5/06/89

File: FUN.LNF
Screen: Dominican Beach
Artist: Cheryl Vince
Cat No: 520-Q983
Date: 3/17/89

The database shown here requires screens that combine text with graphics artwork. *The C-scape interface manager facilitated the design and implementation of the screens and menus. (Photo courtesy Oakland Group)*

or 80486-based computers, EGA-compatible cards, and high-resolution monitors. The company's existing programs, which work perfectly well and have sufficient flexibility to accommodate most of a user's new requirements, would have to be completely rewritten—and programmers who are proficient in working with Windows or Presentation Manager are still a very small minority. Last (but by no means least), all of the users in the company would have to be completely retrained. All of this work amounts to big bucks.

At present, therefore, Tonkin finds that companies who want to increase productivity are reluctant to face the upheavals and expense of installing a GUI. Instead, they're much more likely to upgrade to 80386- or 80486-based PCs or compatibles (still with monochrome displays) to get better processing performance, while retaining the benefits of a familiar operating environment and proven programs.

Because software is the most labor-intensive component of a computer system, it's also the most expensive. For this reason and others (including the issue of reliability), the past 20 years have seen a consistent drive to convert software design from a black art to an engineering discipline. The CASE tools that have appeared have done much to simplify the process of generating specifications from users' requirements, and of converting the specifications into an internally consistent design. At the implementation level, however, most CASE tools can generate only skeleton code in Ada or C. Something more is needed in order to make portions of a design reusable in other, similar systems.

Two approaches can contribute to the creation of reusable modules that will save both coding and testing effort when you come to design similar systems. The most recent, and so far not very widespread approach, is that of object-oriented programming (**Ref 2**). The other approach is to link in from a library predefined, pretested, and sometimes precompiled, routines that accomplish the functions you need.

A good library of routines fulfills the same engineering function as a good hardware inventory of connectors, heat sinks, and machine screws. A hardware engineer doesn't design and fabricate these items unless the application absolutely demands it; likewise, a software engineer should not spend time writing and testing code for low-level functions if those functions are available in a commercial library.

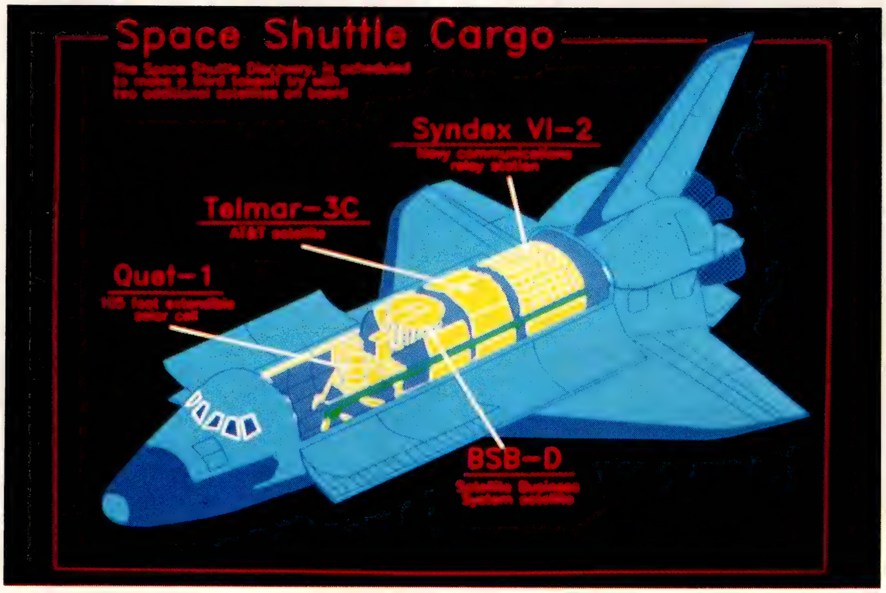
The Modula-2 language has built into it the concept of reusable modules—but not much is available in the way of commercial libraries. Fortran libraries relate mostly to the scientific, mathematical, and statistical fields. Because the language does not lend itself easily to modern graphics, you'd probably have a hard time finding a Fortran graphics library.

If you're designing applications in C for use with IBM PCs and compatibles, there exists a wealth of reliable libraries covering a wide variety of applications, including text manipulation, mathematics, statistics, telecommunications, and graphics. The number and scope of the graphics libraries is increasing almost daily; they cover not only menus and windows for character-based applications, but also routines that will greatly simplify the implementation of graphics-intensive applications that will run under MS Windows or Presentation Manager.

Among the most versatile of the libraries is the Graphics Development Toolkit from Graphic Software System Inc (GSS). There are two versions of this $595 tool set, one for PC-DOS and the other for OS/2. Each of them gives you access to more than 100 high-level graphical functions with a consistent interface to more than 300 different graphical devices. The functions fall into 17 groups that include dynamic loading; workstation control; lines and arcs; polygons, circles, bars, and other shapes; polymarkers;

bitmap operations; pixel arrays; graphics text; clipping; and error handling. Further, you can link the routines to programs written in C, Fortran, Pascal, or Microsoft compiled Basic.

Another widely used development tool set is Halo from Media Cybernetics. There are three versions of this kit: the basic kit ($395), which provides 200 graphics subroutines and works with more than 180 graphics I/O devices as well as scanners and high-resolution imaging boards; the $595 window tool kit, which has all of the basic features but also provides command bars, pull-down menus, scroll bars, radio buttons, and icons; and the $695 OS/2 version, which adds multithread, multitasking capabilities, a dynamic-link library, and background-mode graphics. All three versions work with the Microsoft C compiler. In addition, the basic kit has interfaces to 17 other compilers.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Satellite Business System satellite

You can mix graphics and text on the screen, *using only the high-level commands of the Graphics Development Toolkit. (Photo courtesy GSS)*

The Oakland Group's C-scape combines the two approaches mentioned earlier: It uses object-oriented programming techniques, which let you create customized, reusable code modules. It also provides access to a variety of low-level subroutines with interfaces to PC-DOS, OS/2, and Unix. Your applications built with C-scape will automatically detect the presence of CGA, EGA, VGA, or Hercules boards. You can choose from pop-up, tiled, bordered, or exploding windows. You can also link context-sensitive help messages to individual screens or fields. The basic C-scape costs $299; an optional Look-and-Feel module ($149) lets you build any type of screen or form and automatically converts your design to C source code. The two modules together cost $399. Prices for Unix, Xenix, and other Unix derivatives start at $999.

South Mountain Software's Essential Graphics ($299) is an upgrade of a well-known and widely used C library and now includes 3-D multiview, multiperspective capabilities. This library provides more than 300 functions for use with 8514, VGA, EGA, CGA, Hercules, and other graphics boards. You can direct the output to dot-matrix printers, Hewlett-Packard laser printers, and pen plotters. Input devices include scanners, light pens, and digitizers. The library is compatible with Microsoft C, Turbo C, and Lattice C compilers.

There are two CASE tools from CaseWorks that are specifically directed toward facilitating application-program development under either MS Windows (CASE:W, $795) or the OS/2 Presentation Manager (CASE:PM, $995). Each of these tools consists of two mod-

For more information . . .

For more information on the graphics libraries discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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CIRCLE NO. 90

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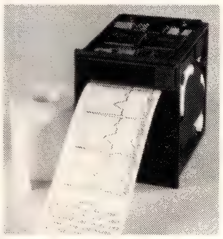

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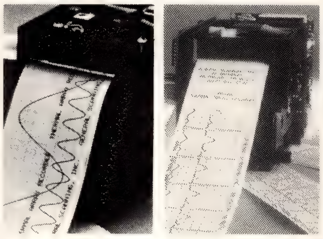

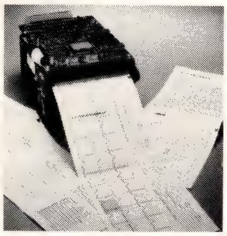

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ules. The prototyper elicits from you information about each type of screen that you want, such as the number of menu items, and what the menu items should do, together with color and menu size. When you've finished the prototype phase, your screens are defined by C source code that you can link to dialogue boxes or to your own code.

The generator uses knowledgebase techniques to generate C source code that you can compile to a stand-alone executable program. The generator also elicits from you information about other compilable files and creates a make file that constructs the whole system for you. The package has a regeneration capability that preserves your source code so that you can modify it and then regenerate the system. This feature is valuable because many screen generators meld your application code so inextricably with the graphics code that modifications effectively require you to start the prototyping phase over from scratch.

These examples are only a few of the most recent additions to the graphics library field. Time you spend perusing advertisements for other graphics libraries will be time well spent. You're almost sure to find a graphics library or development system that will meet your needs and save you from having to learn the quirks of the 450 or so functions of Windows and many more for Presentation Manager.

EDN

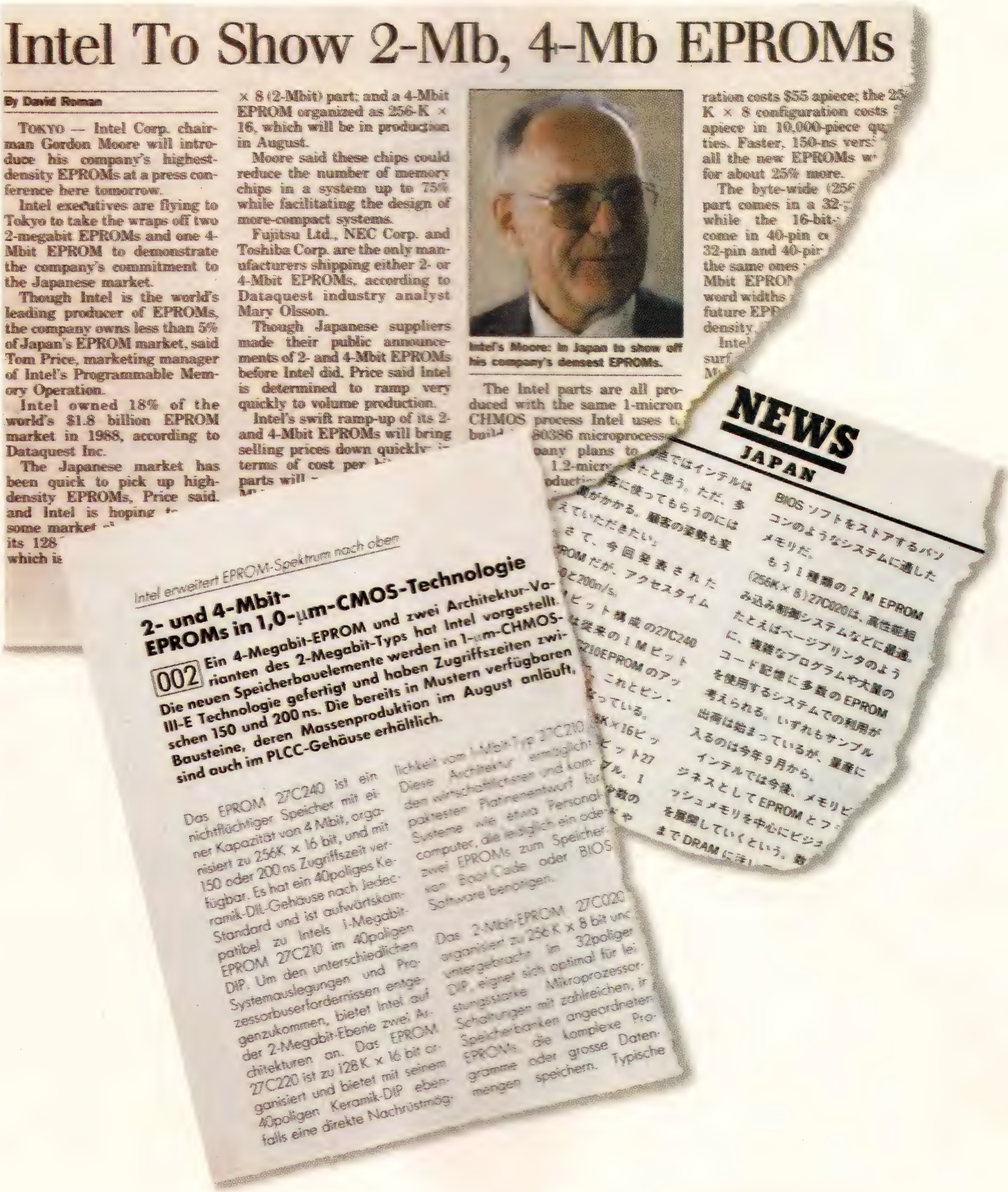
References

1. Tonkin, Bruce, "GUI, Phooey!" *Computer Language*, November, 1989, pg 157.

2. Terry, Chris, "Objects facilitate modular, reusable code," *EDN*, November 9, 1989, pg 85.

Article Interest Quotient
(Circle One)
High 509 Medium 510 Low 511

Now that we've been properly introduced,



Intel To Show 2-Mb, 4-Mb EPROMs

By David Roman

TOKYO — Intel Corp. chairman Gordon Moore will introduce his company's highest-density EPROMs at a press conference here tomorrow.

Intel executives are flying to Tokyo to take the wraps off two 2-megabit EPROMs and one 4-Mbit EPROM to demonstrate the company's commitment to the Japanese market.

Though Intel is the world's leading producer of EPROMs, the company owns less than 5% of Japan's EPROM market, said Tom Price, marketing manager of Intel's Programmable Memory Operation.

Intel owned 18% of the world's $1.8 billion EPROM market in 1988, according to Dataquest Inc.

The Japanese market has been quick to pick up high-density EPROMs, Price said, and Intel is hoping
some market
its 128
which is

× 8 (2-Mbit) part; and a 4-Mbit EPROM organized as 256-K × 16, which will be in production in August.

Moore said these chips could reduce the number of memory chips in a system up to 75% while facilitating the design of more-compact systems.

Fujitsu Ltd., NEC Corp. and Toshiba Corp. are the only manufacturers shipping either 2- or 4-Mbit EPROMs, according to Dataquest industry analyst Mary Olsson.

Though Japanese suppliers made their public announcements of 2- and 4-Mbit EPROMs before Intel did, Price said Intel is determined to ramp very quickly to volume production.

Intel's swift ramp-up of its 2- and 4-Mbit EPROMs will bring selling prices down quickly
terms of cost per
parts will

Intel's Moore: In Japan to show off his company's densest EPROMs.

The Intel parts are all produced with the same 1-micron CHMOS process Intel uses to
build 80386 microprocess
pany plans to
1.2-micr
producti

ration costs $55 apiece; the 25
K × 8 configuration costs
apiece in 10,000-piece qu
ties. Faster, 150-ns vers
all the new EPROMs w
for about 25% more.

The byte-wide (256
part comes in a 32-
while the 16-bit
come in 40-pin c
32-pin and 40-pi
the same ones
Mbit EPRO
word widths
future EP
density,

Intel
surf
M

Intel erweitert EPROM-Spektrum nach oben

2- und 4-Mbit-EPROMs in 1,0-µm-CMOS-Technologie

002 **Ein 4-Megabit-EPROM und zwei Architektur-Varianten des 2-Megabit-Typs hat Intel vorgestellt. Die neuen Speicherbauelemente werden in 1-µm-CHMOS-III-E Technologie gefertigt und haben Zugriffszeiten zwischen 150 und 200 ns. Die bereits in Mustern verfügbaren Bausteine, deren Massenproduktion im August anläuft, sind auch im PLCC-Gehäuse erhältlich.**

Das EPROM 27C240 ist ein nichtflüchtiger Speicher mit einer Kapazität von 4 Mbit, organisiert zu 256K × 16 bit, und mit 150 oder 200 ns Zugriffszeit verfügbar. Es hat ein 40poliges Keramik-DIL-Gehäuse nach Jedec-Standard und ist aufwärtskompatibel zu Intels 1-Megabit-EPROM 27C210 im 40poligen DIP. Um den unterschiedlichen Systemauslegungen und Prozessorbuserfordernissen entgegenzukommen, bietet Intel auf der 2-Megabit-Ebene zwei Architekturen an. Das EPROM 27C220 ist zu 128K × 16 bit organisiert und bietet mit seinem 40poligen Keramik-DIP ebenfalls eine direkte Nachrüstmöglichkeit vom 1-Mbit-Typ 27C210. Diese Architektur ermöglicht den wirtschaftlichsten und kompaktesten Platinenentwurf für Systeme wie etwa Personalcomputer, die lediglich ein oder zwei EPROMs zum Speicher von Boot-Code oder BIOS-Software benötigen.

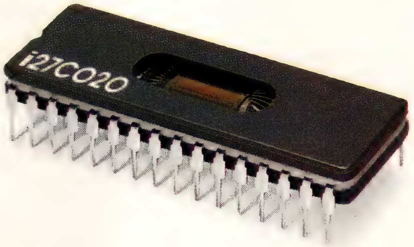
Das 2-Mbit-EPROM 27C020 organisiert zu 256 K × 8 bit und untergebracht im 32poliger DIP, eignet sich optimal für leistungsstarke Mikroprozessor-Schaltungen mit zahlreichen, in Speicherbanken angeordneten EPROMs die komplexe Programme oder grosse Datenmengen speichern. Typische

NEWS
JAPAN

ではインテルは
きたと思う。ただ、多
客に使ってもらうのには
間がかかる。顧客の姿勢も変
えていただきたい」
さて、今回発表された
ROMだが、アクセスタイム
と200n/s。
ビット構成の27C240
は従来の１Mビット
210EPROMのアッ
。これとピン、
っている。
K×16ビッ
ビット27
ブル。１
数の
や

BIOSソフトをストアするパソ
コンのようなシステムに適した
メモリだ。
もう１種類の２M EPROM
(256K×8)27C020は、高性能組
み込み制御システムなどに最適。
たとえばページプリンタのよう
に、複雑なプログラムや大量の
コード記憶に多数のEPROM
を使用するシステムでの利用が
考えられる。いずれもサンプル
出荷は始まっているが、量産に
入るのは今年９月から。
インテルでは今後、メモリビ
ジネスとしてEPROMとフ
ッシュメモリを中心にビジ
を展開していくという。
までDRAMに注

take me home.



Recently, we announced our commitment to 2- and 4-Mbit EPROMs. And now, we're shipping our 2-Mbit EPROMs in volume. With our 4-Mbit EPROMs right behind them.

But, this high-speed ramp should hardly come as a surprise. After all, we invented the EPROM and have always been the volume leader.

And we've produced this latest generation with the same proven 1-micron CHMOS*IIIE process as our 1-Mbit EPROMs. So we can deliver 2-Mbit production quantities in no time at all.

As you can see from the chart, we're the EPROM source you've been looking for. Only Intel gives you the widest range of densities, from 16K to 4-Mbit. And that's just the beginning. We also let you choose byte-wide or word-wide architectures. PLCC or CERDIP packaging. And a range of speeds, from 120 ns to 200 ns.

But whichever Intel EPROM you choose, the benefits are obvious. Using one 2-Mbit instead of eight 256K EPROMs, for example, results in reduced board space, increased system reliability and

---

*CHMOS is a patented process of Intel Corp.

overall lower system cost.

Our 1- and 2-Mbit EPROMs are available today in whatever quantity you need. More importantly, our 1-Mbits are your most cost-effective solution now, followed by our 2-Mbits in 1990. Or you can design in our 4-Mbit EPROMs today. They'll be available in full volume and in a full range of configurations for your next generation of products.

Available in Volume	Product	Organization	Pins	Package
1-Mbit	27C010	128K × 8	32	CERDIP
	27C010	128K × 8	32	PLCC
	27C210	64K × 16	40	CERDIP
	27C210	64K × 16	44	PLCC
2-Mbit	27C020	256K × 8	32	CERDIP
	27C220	128K × 16	40	CERDIP
4-Mbit	27C240	256K × 16	40	CERAMIC

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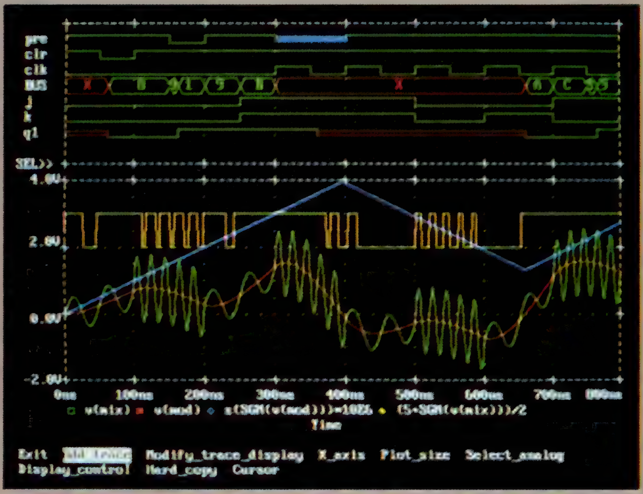
MicroSim Corporation

The Standard for Circuit Simulation



Analog and digital waveforms with common time axis

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Two years ago, MicroSim introduced the technology for simulating mixed analog/digital circuits. Now, this capability is available in the Digital Simulation extension for PSpice. It does true mixed-mode simulation of circuits – including feedback loops between analog and digital sections.

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CIRCLE NO. 93

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Peripheral turns pocket-size computer into data-acquisition system

A 2.75×4×1-in., 6-channel analog/digital data-acquisition unit appears to be the first third-party peripheral for Atari Corp's minuscule Portfolio computer—the $399.95, 1-lb, handheld CPU that runs a large amount of IBM PC software. The Palmdac clips onto the side of the Portfolio and draws power either from a wall-mounted transformer or from the three alkaline AA cells that power the CPU.

Included in the data-acquisition unit are a 12-bit ADC, which can take 1024 samples/sec, two differential channels with a full-scale range (FSR) you can set to 25 or 250 mV, and four single-ended channels that have an FSR of 2.5V. You can also connect this second group of channels as two differential inputs or as one differential- and two single-ended inputs. In addition, the unit includes a programmable timer that initiates data sampling either 2, 4, 8, 16, 32, 64, 128, 256, or 1024 times/sec, or 1 time/minute, 1 time/day, or 1 time/month.

An unusual feature is the transducer-excitation capability; the unit includes a pair of 2.5V dc sources, each of which can supply 10 mA max. To preserve battery power, you can switch these sources on and off under software control—furnishing excitation to external transducers only while the unit is scanning their outputs.

A fresh set of batteries will run the computer and the data-acquisition unit continuously for a minimum of eight hours. If you power the data-acquisition unit from the ac line, and ac power fails, the computer continues to operate.

The vendor furnishes the data-acquisition control software on an IBM PC-compatible floppy disk. You can use the standard PC's printer port and the Portfolio's $49.95 parallel port or the standard PC's serial port and the Portfolio's RS-232C port ($79.95) to download the software into the Portfolio's main memory. As an alternative, you can copy the software to a credit-card-size battery-backed RAMdisk that you then plug into the Portfolio. These cards, with capacities from 32k to 128k bytes, ($79.95 to $199.95) retain data for 10 years. A $99.95 Atari peripheral for standard PCs reads and writes the RAMdisk cards.

The Palmdac, a diminutive data-acquisition unit, *attaches to the side of Atari Corp's tiny Portfolio computer to create a portable 6-channel data logger that you can operate from the computer's internal batteries.*

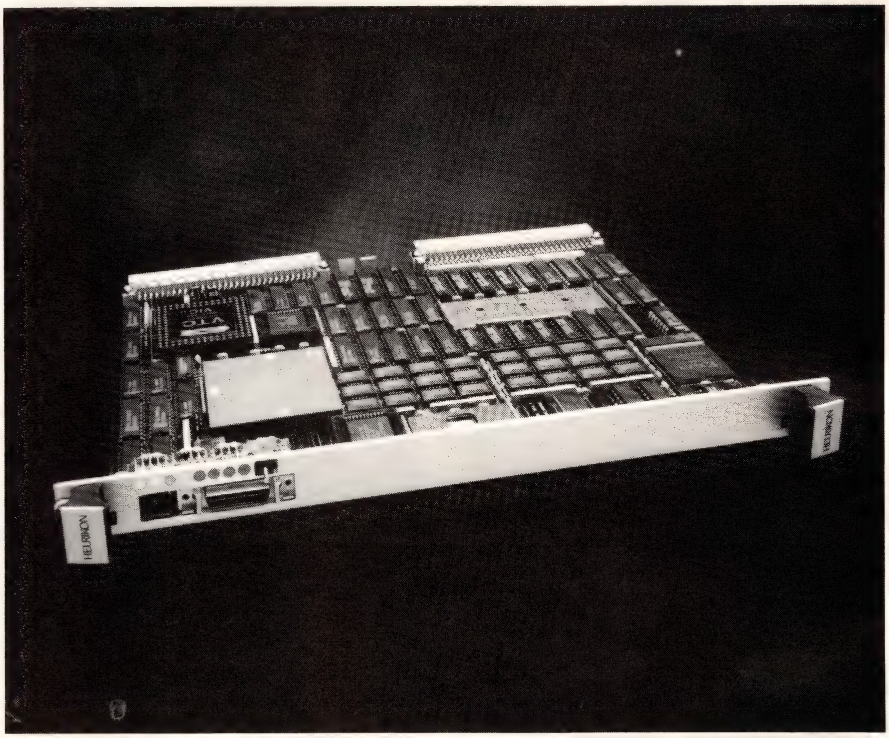
The data-acquisition software scales the acquired data and displays it in engineering units on the Portfolio's 8-line by 40-character screen. To conserve memory, the software stores the data in binary form. You can use any of the mechanisms for software downloading described above to retrieve acquired data from the Portfolio. Once you have the data in the standard PC, you can load it into a great many data-reduction and analysis programs. The Palmdac sells for $295. Delivery is 60 days ARO.

—Dan Strassberg

Microprocessor Designs, 61 Falls Rd, Shelburne, VT 05482. Phone (802) 985-2535.

Circle No. 730

VMEbus CPU card hosts a 68040 µP and includes a 200M-byte/sec local bus



VSB support and the 200M-byte/sec Corebus *make the 68040-based HK68/V4F VMEbus CPU card customizable for a wide range of applications.*

The Model HK68/V4F VMEbus CPU card, based on the new Motorola 68040 µP, includes a 50-MHz, 200M-byte/sec, synchronous local-bus interface called Corebus. The Corebus serves to connect the onboard CPU, memory, and I/O subsystems, and it provides expansion capability via daughter cards. The VMEbus card also includes an industry-standard VSB interface with master/slave support.

Standard features of the HK68/V4F include 2M to 8M bytes of 70-nsec, 2-way-interleaved static-column dynamic RAM and as much as 2M bytes of EPROM. The board also includes 512 bytes of nonvolatile RAM that can store configuration information. An additional 960M bytes of memory are addressable via the VSB interface. I/O capabilities include two RS-232C ports and an optional RS-422 port. You can add support for Ethernet or SCSI via Corebus cards.

The VMEbus Interface Consortium's VIC068 IC provides the main bus interface and allows the card to support 40M-byte/sec transfers. The interface chip supports seven bus interrupts and master-and-slave operation, and it includes system-controller functions such as 4-level arbitration. The board also includes two counter timers, a real-time clock, and a power-fail indicator.

The card is upward object-code compatible with boards based on the 68020 µP and 68881/68882 FPU (floating point unit). The 68040 includes 4k-byte instruction and data caches on chip, as well as a paged memory-management unit with dual 64-entry, 4-way, set-associative translation lookaside buffers.

The Corebus expansion bus operates synchronously at 50 MHz and supports burst transfers as fast as 200M bytes/sec. The bus design actually includes both the Module Synchronous Bus, which supports high-speed multimaster capabilities, and the 16-MHz Asynchronous Peripheral Bus. The two buses share data and address lines and allow the designer to match the cost and performance requirements of different expansion applications. The company plans to submit the specification for Corebus to VITA (VMEbus International Trade Association) for consideration as an industry standard.

Software support for the HK68/V4F includes the Unix, OS-9, VRTX, and VxWorks operating systems. You can use the boards as development hosts and as real-time target systems. A 25-MHz version of the board with 2M bytes of memory costs $3495 and will be available in the second quarter.

—Maury Wright

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Circle No. 731

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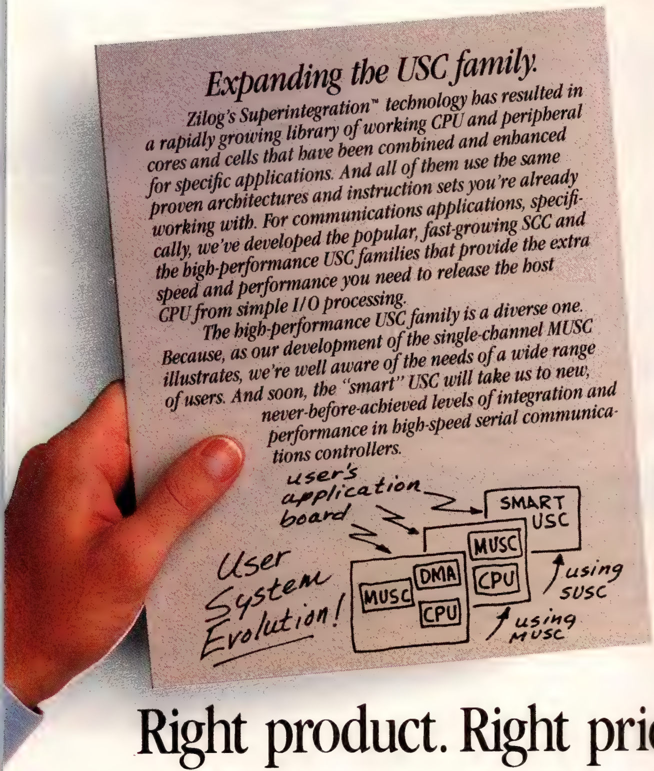
All the flexibility you need.

The MUSC's multiprotocol design lets you adapt your system to a variety of networks. But not only do you get 10 protocols, you get 8 encoding formats—including asynchronous, bit and byte synchronous, isochronous, Ethernet, and MIL-STD 1553B. And the Open Systems Interconnect (OSI) model features Time Slot Assignment that allows transmission of time multiplexed Synchronous Data Link Control (SDLC) protocol to the ISDN link level.

All the reliability you've come to expect.

Of course, the MUSC comes to you off the shelf, with Zilog's proven quality and reliability. And you have the advantage of CMOS and Superintegration. But you also have the MUSC's unique built-in bus-oriented testability, which allows access to nodes and registers for testing program functionality in real time. And, since dedicated pointer registers provide a window to serial flow during on-line testing, you can test transmission reliability of the controller during system operation.

To find out more about the MUSC or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.



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The high-performance USC family is a diverse one. Because, as our development of the single-channel MUSC illustrates, we're well aware of the needs of a wide range of users. And soon, the "smart" USC will take us to new, never-before-achieved levels of integration and performance in high-speed serial communications controllers.

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CIRCLE NO. 94

THE NEXT TIM A DATA ACQUIS GEOSEISMI FLIGHT SIMU AND YOU NEED CALL

Ok, so you've got a project that needs a quick and reliable memory subsystem that can accomplish the impossible. The first call you make is home. You're going to be a little late.

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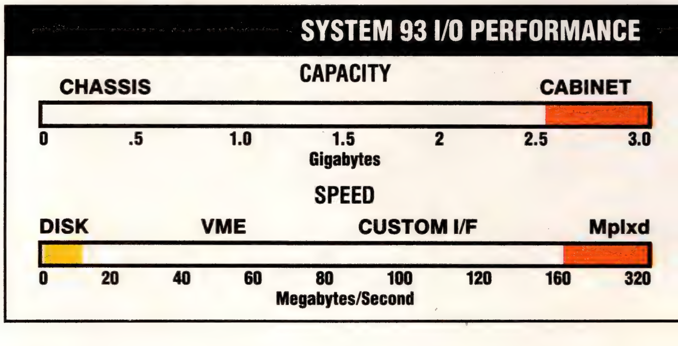

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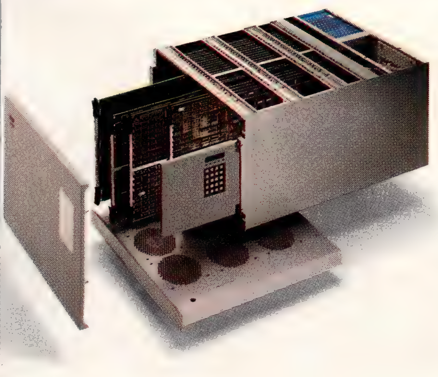

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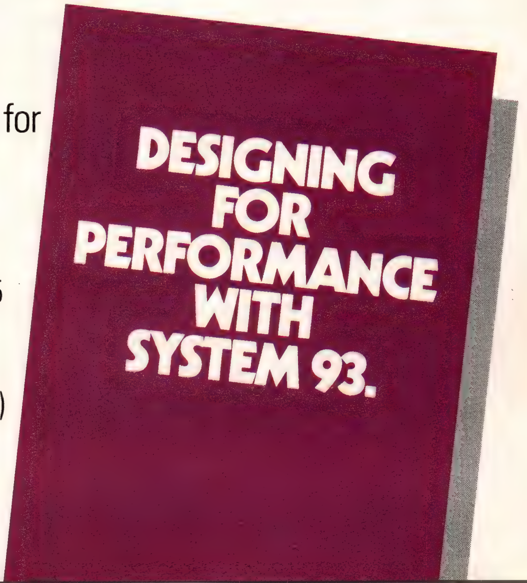


CIRCLE NO. 95

Static RAMs

As processing speeds exceed 30 MHz, the memory devices in your system pose design problems of their own. At these speeds, traces act like transmission lines, so reflections, ground bounce, crosstalk, and signal degradation all become critical factors in your design.

If you face designing or upgrading a system that includes one of today's high-speed CPUs, you may discover that the transition from 70- to 35-nsec memories was much simpler than the transition from 35- to 15-nsec devices. To get stable and reliable signal transmissions when using static RAMs (SRAMs) that sport access times of 15 nsec or less, you'll have to take RF and transmission-line theory into consideration to reduce the resultant increase in system noise. Timing factors, trace routes, pc-board construction, line lengths, power distribution, and heat dissipation all affect your system's noise levels. Memories could interpret higher levels of noise as data, thus corrupting its contents. The noise generated within your system may have presented no problem for slower SRAMs, but the edge rates of a 15-nsec TTL CMOS SRAM make the part much more susceptible to false triggering.

The low-power and high-speed characteristics of CMOS ICs make them the popular choice among system designers. As a result, most of the SRAMs offered today are CMOS parts with TTL voltage-output levels. But to gain better noise immunity, you may have to leave your comfort zone and investigate BiCMOS devices or even resort to ECL memories.

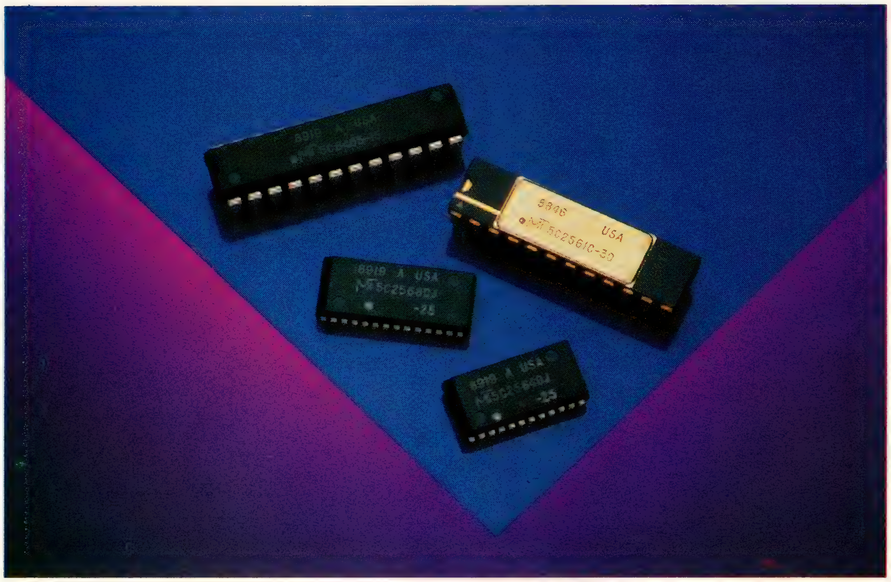
BiCMOS parts combine CMOS internal transistors and bipolar I/O transistors to reduce output voltage swings. The CMOS guts, of course, allow greater circuit densities than would a strictly bipolar part. The bipolar components of BiCMOS memories offer I/O compatibility with standard TTL or ECL levels. The bipolar aspects also reduce propagation delays, increase the chip's resistance to ground-bounce

J D Mosley, *Regional Editor*

EDN SPECIAL REPORT

***As static RAMs (SRAMs) zoom** to ever-higher speeds, you'll have to take steps to reduce the increased level of noise in your designs. (Photo courtesy Micron Technology Inc)*

You'll have to take RF and transmission-line theory into consideration when using SRAMs that have access times of 15 nsec or less.

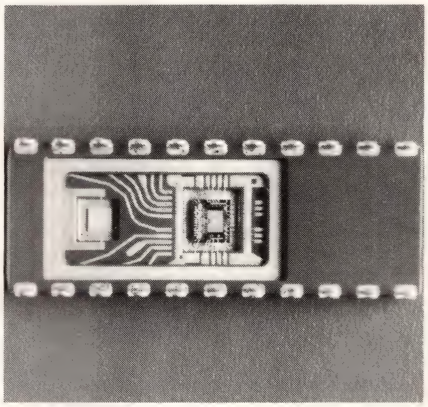


***Because DIP and surface-mount packages** are available for virtually every SRAM, you can select from a variety of packaging options to meet your design parameters. These SOJs and DIPs represent the more popular options available from Micron Technology.*

problems, and provide greater noise immunity. However, BiCMOS parts are not as widely available as CMOS memories, as manufacturers continue to develop and fine-tune their BiCMOS fabrication processes.

If you need more noise immunity and performance greater than BiCMOS SRAMs offer, consider ECL devices. Unlike voltage-driven TTL chips, current-driven ECL chips aren't susceptible to ground-bounce problems and have lower impedances and voltage swings. Because they use differential amplifiers to prevent transistor saturation, ECL SRAMs have faster switching speeds with smaller signal swings compared with TTL parts. Accordingly, systems with ECL memories are typically an order of magnitude quieter than their TTL-laden counterparts. ECL also provides high fan-out and can readily drive low-impedance transmission lines. An example of a high-performance ECL SRAM is Cypress Semiconductor's 3.5-nsec 4k-bit CY10/100E474. A 3-nsec version will be available during the first quarter of this year.

ECL SRAMs have signal levels defined as 10k, 100k, or a recent category that manufacturers refer to as 101k. The 100k memories operate from a −4.5V supply; the 101k and 10k SRAMs operate from a −5.2V supply. The higher supply voltage lets 101k parts draw more current than the 100k parts, which results in faster data-transfer rates and higher alpha-particle immunity than equivalent 100k SRAMs. The 10k devices are temperature compensated. The 100k and 101k parts have both voltage and temperature compensation.

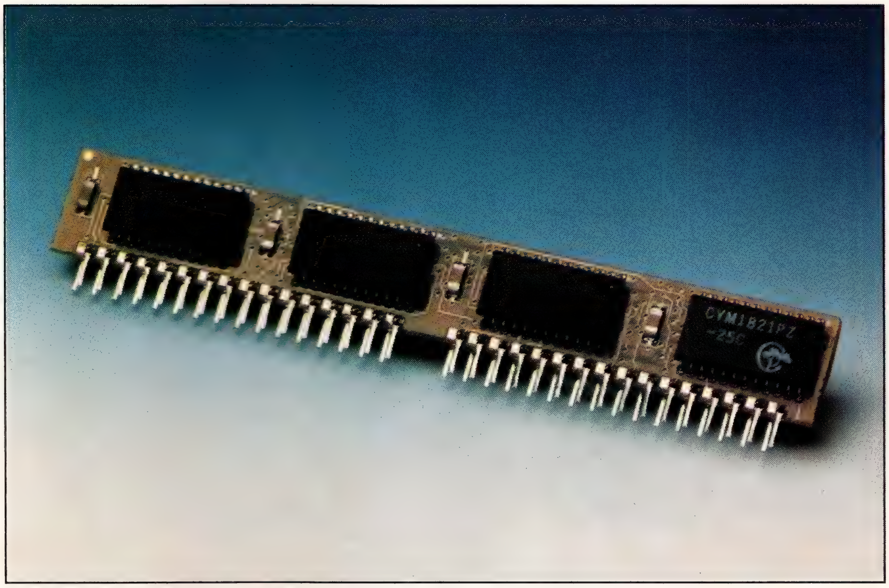


***Featuring a 3-nsec access time** and providing inherent radiation hardness, the VS12G422T GaAs SRAM from Vitesse also provides TTL compatibility and operates from a standard 5V supply.*

The major drawbacks of ECL SRAMs are incompatibility with TTL voltage levels, their relative scarcity, and the fact that many engineers are unfamiliar with the ECL design spec. You aren't likely to run into serious design problems if you drive 100k inputs with 10k outputs. But if you try driving 10k inputs with 100k outputs, the 10k part may not be able to distinguish a high level from the 100k driver. To increase the noise margin between 10K and 100K parts, you must keep the system's temperature under 35°C. National Semiconductor offers a series of application notes that contain many helpful hints, such as this one, for using ECL BiCMOS SRAMs.

Another drawback of ECL SRAMs is that prices for ECL parts are typically slightly greater than for their TTL counterparts. This price difference is primarily due to supply-and-demand tradeoffs stemming from the greater availability of TTL devices. For example, Fujitsu's 15-nsec 256k-bit ECL MBMC500-15 sells for $87.50 (1000) in ceramic DIPs—a price that's significantly higher than Hitachi's $39.80 (1000) 15-nsec HM6709A. However, when you consider the improved noise immunity you get with ECL, any initial price premium you pay may be offset many times by the savings in engineering costs for your next system upgrade to higher-performance memories.

Regardless of the fabrication methods used in manufacturing your SRAMs, you must still keep RF design factors in mind to reduce the noise caused by faster parts. Take extra pains to minimize the length of the traces on your pc board. Try to use rounded trace angles and avoid right-angle traces. Separate the signal source and its load by the shortest possible path, so that the trace adds a minimum of series inductance and shunt capacitance. Trace length is such a critical factor in high-speed systems for reducing reflections that many designers have switched to surface-mount technology. By using surface-mount components, you can have devices on both sides of your board and significantly reduce trace lengths.



SRAM modules help you increase *the amount of memory you can squeeze onto your board. This 512k-bit module from Cypress contains eight 16k×4-bit SRAMs in SOJ packages mounted on an epoxy laminate board. This configuration provides a 32-bit-wide data path, which isn't yet available in 512k-bit monolithic memories.*

Route critical signals, such as the clock, between the power and ground planes to reduce crosstalk. By isolating the clock in this manner, you can improve overall system reliability. If the clock degrades, so does the whole system.

Another factor in reducing system noise is proper line termination. You can overburden your circuit's capacitance-loading requirements when the μP, the coprocessors, and cache memory all run on the same bus. Look for SRAMs that have a high (80- to 100-pF) capacitive rating and check for impedance mismatches that will create reflections and cause false-timing problems. Make an effort to accurately assess all the timing specs of the components in your circuit and relate them to the timing requirements of your processors and interfaces. This assessment is particularly tricky, since no guidelines exist to standardize timing specs among manufacturers. Analyze the SRAM's behavior over the full operating temperature range and determine whether you'll need to force air through the system for heat dissipation. One easy way to analyze chips over the operating temperature range of your system is to take advantage of Motorola's free sample pack of eight 12-nsec 64k-bit SRAMs.

Besides problems that individual components can cause, you should consider the circuit board. To control the line impedance of your circuit board, you must control the thickness and width of the traces as well as the distance of each trace from the ground plane. You can minimize problems with capacitive loading by using separate in-phase clocks for each processor and coprocessor on your board. Make sure the lengths of all bus lines are equal.

Power distribution can also affect the noise levels of your design. Noise in the power-supply voltage or in your circuit's supply lines reduces the circuit's overall noise margin and makes your circuit more susceptible to crosstalk and ringing. Decoupling capacitors will help you maintain the highest amount of ac attenuation possible—the lower the ground impedance, the better the decoupling capacitors can act as line filters. Make sure you consider the total voltage drop on the circuit's power buses and eliminate external sources of noise. Beware of separate power supplies that are inadequately grounded or have common positive terminals at different potentials. Minimize current fluctuations within the circuit.

When selecting an SRAM, identify all its critical parameters, such as output enable, rather than just looking for raw-brute-force access time. Carefully consider address and data setup times. Output enable and write-pulse width are critical SRAM factors that may be even more important than access times when determining system perform-

Text continued on pg 132

Table 1—Representative static RAMs

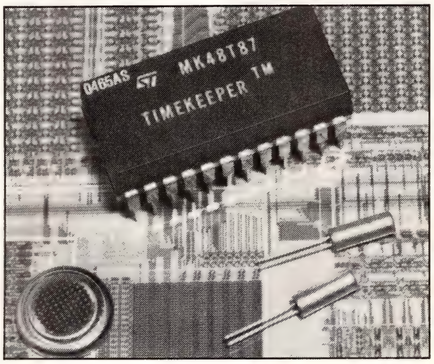
Company	Part number	Fabrication process	Bits	Access time (nsec)	Organization (bits)	Price
Alliance	AS7C164	CMOS	64k	25/35/45/55/70	8k×8	$3 to $10
	AS7C186	CMOS	64k	20/25/30/35/45	16k×4	$3 to $10
	AS7C256	CMOS	256k	25/35/45/55/70	32k×8	$3 to $10
Cypress	CYM1641	CMOS	4M	25/30/35/45/55	64k byte×32 bit	$803 (35 nsec)
	CYM1830	CMOS	2M	25/30/35/45/55	64k byte×32 bit	$803 (35 nsec)
	CY7C189	CMOS	64	15	16×4	$7.80 (100)
	CY7B161/162/164/166	BiCMOS	64k	10/12/15	8k×8	$20 to $80
	CY10/100E494	BiCMOS	64k	3/5/7/10/12	16k×4	$8.95 to $95
Dallas Semiconductor	DS1244	CMOS	256k	120	32k×8	$35 (100)
	DS1245	CMOS	1M	100/120	128k×8	$95 (100)
Fujitsu	MBM100C504	BiCMOS	256k	15	64k×4	$87.50 (1000)
	MBM10486 LL-13/RR-13/ RL-13	Bipolar	16k	13	4k×4	$53.50 (1000)
Harris	HS-65T162RH	CMOS	16k	120	2k×8	$800 (100)
Hitachi	HM6208H	CMOS	256k	25/35	64k×4	$14
	HM6709A	BiCMOS	256k	15/20	64k×4 with output enable	$39.80 (1000 qty; 15 nsec)
	HM10504	BiCMOS	256k	10/12	64k×4	$185 (1000)
	HM624257	CMOS	1M	35/45	256k×4	$90
Logic Devices	LMM4016	CMOS	4M	25	256k×16	$288 (OEM qty)
	L7C174	CMOS	64k	15	8k×8	$49.50 (100)
	L6116	CMOS	16k	10	2k×8	$21.35
Matra MHS	65764	CMOS	64k	25/35/45/55	8k×8	$5 to $6
Micron Technology	MT5C1627	CMOS	16k	100	2k×8	<$5
	MT5C6408	CMOS	64k	12/15/20/25/30	8k×8	$13
	MT5C2568	CMOS	256k	20/25/30/35	32k×8	$30
	MT5C1005	CMOS	1M	25/35	256k×4 with output enable	$175
	MT85C3264	CMOS	2M	25/30/35/45	64k×32	$400
Mitsubishi	M5M21C68	CMOS	16k	45/55	4k×4	$3.50
	M5M5258B	CMOS	256k	15/20	64k×4	$35 to $45
	M5M51001	CMOS	1M	35/45	1M×1	$120 to $180
	M5M1008	CMOS	1M	70/85/100/120	128k×8	$95 to $128
Motorola	Quickram family	CMOS	64k to 288k	12 (64k) to 20 (288k)	×1, ×4, ×8, ×9	$24 to $147
	DSPRAM	HCMOS	192k	25/30/35	8k×24	$37 (100 qty; 25 nsec)
	MIPS R3000 series	HCMOS	256k	20	16k×16	$66 (100)
National Semiconductor	NM100500	BiCMOS III	256k	15/18	256k×1	$125 (1000 qty; 15 nsec)
	NM5104	BiCMOS III	256k	12/15	64k×4	$175 (1000 qty; 12 nsec)
	NM10494	BiCMOS III	64k	10/12/15	16k×4	$115 (100 qty; 10 nsec)
Paradigm	PDM41251S/L	CMOS	256k	15/20/25/35/45/55	64k×4	$94 (100 qty; 15 nsec)
	PDM41256S/L	CMOS	256k	20/25/35/45/55	32k×8	$104 (100 qty; 15 nsec)
SGS-Thomson Microelectronics	MK41H80	HCMOS 3	16k	12 to 25	4k×4	$18.75 (1000 qty; 20 nsec)
	MK48H64	HCMOS 3	64k	70 to 120	8k×8	$5.93
	MK48Z08B55	HCMOS 3	64k	55	3k×8	$23 (1000)
Simtek	STK10C68A	Novcel	64k	35/45/55	8k×8	$28.77 to $48.30 (1000)
Sony	CXK7701J	CMOS	32k	30/35/45/55	8k×16 or two 4k×16	$64.20 (30 nsec); $50 (35 to 55 nsec)
	CXK581020	CMOS	1M	35/45/55	128k×8	$300 to $416.70 (100)
Texas Instruments	SMJ61CD16LA/SA	EPIC	16k	25/35/45/55/70	16k×1	$21 (100 qty; 35 nsec)
	SMJ61CE256L/S	EPIC	256k	35/45/55/70	32k×8	$130 (100 qty; 35 nsec)
Toshiba	TC5589P/J-15/-20/ -25/-35	CMOS	73, 728	15/20/25/35	8k×9	$6.55 (1000 qty; 35 nsec)
	TC518129AFWL -80LV/-10LV/-12LV	CMOS	1M	80/100/120	128k×8	$15.95 (1000 qty; 12 nsec)
Vitelic	V61C16	CMOS	16k	35 to 70	2k×8	$2 (35 nsec)
	V63C64	CMOS	64k	25 to 55	8k×8	$8 (25 nsec)
	V63C330	CMOS	128k	25/35/45	8k×16	$38 (25 nsec)
Vitesse	VS12G422T	GaAs E/D MESFET	1024	5/6/8	256×4	$29 to $52
	VS12G422E	GaAs E/D MESFET	1024	4/5	256×4	$32 to $45
	VS12G476	GaAs E/D MESFET	4096	3/4/5	1024×4	$64 to $82
VLSI Technology	VT20C19/69/79	CMOS	16k	12/15	2k×8/4k×4	$14.85 (100)
	VT62A168/188	CMOS	144k/128k	25/35	8k×16/8k×18	$35 (100)
	VT624256	CMOS	1M	35/45	256k×4	$231.25 (100)

Packages	Feature size (μm)	Power consumption (active/standby)	Input voltage		Output voltage		Special features
			V_{IH} (min)	V_{IL} (max)	V_{OH} (min)	V_{OL} (max)	
DIP, SOJ	1.0	550 mW/110 mW	2.2	0.8	2.4	0.4	2V data-retention option
DIP, SOJ	1.0	440 mW/110 mW	2.2	0.8	2.4	0.4	2V data-retention option
DIP, SOJ	1.0	550 mW/110 mW	2.2	0.8	2.4	0.4	2V data-retention option
600-mil DIP	0.8	7.2W (max)	2.2	0.8	2.4	0.4	Configurable ×4-, ×8-, ×16-bit-wide module
600-mil DIP	0.8	4.8W (max)	2.2	0.8	2.4	0.4	32-bit-wide module
16-pin 300-mil DIP	1.2	495 mW (max)	2.0	0.8	2.4	0.45	Inverting and noninverting outputs
DIP, SOJ, LCC	0.8 CMOS, 1.0 Bipolar	575 mW/150 mW	2.2	0.8	2.4	0.4	Mil spec; automatic power-down when deselected
DIP, LCC, flatpack, SOJ, PLCC, LCC	0.8 CMOS, 1.0 Bipolar	1.43W/600 mW	–1.17	–1.48	–1.025	–1.62	Mil spec; balanced read/write cycles
32-pin DIP	0.8	425 mW (max)	2.2	0.8	2.4	0.4	Nonvolatile; automatic-protection circuitry; clock/calendar
32-pin DIP	0.8	425 mW (max)	2.2	0.8	2.4	0.4	Nonvolatile; automatic-protection circuitry
32-pin LCC, 28-pin flatpack	1.2	550 mW/110 mW	2.2	0.8	2.4	0.4	Voltage and temperature compensation
28-pin DIP	1.0	1.08W (max)	–1.165	–1.475	–1.025	–1.62	Self-timed; voltage and temperature compensation
24-pin DIP, flatpack, 32-pin LCC	2.0	385 mW (max)	2.2	0.8	2.4	0.4	Mil spec; rad hard
DIP, SOJ	1.0	1.0W	2.2	0.8	2.4	0.4	Low-power version available
DIP, SOJ	1.0	400 mW (typ)	2.2	0.8	2.4	0.4	
32-pin DIP, 28-pin flatpack	1.0	620 mW	–1.145	–1.45	–1.0	–1.625	
32-pin SOJ	0.8	1.0W	2.2	0.8	2.4	0.4	Low-power version available
48-pin DIP	N/A		2.2	0.8	2.4	0.4	
DIP, SOIC	0.9		2.2	0.8	2.4	0.4	
DIP, SOIC, SOJ	0.9	260 mW/12.5 μW	2.2	0.8	2.4	0.4	
DIP, SOIC, SOJ	0.8	500 mW (max)	2.2	0.8	2.4	0.4	ESD protection >2000V
28-pin DIP, SOJ	1.2	385 mW (max)	2.2	0.8	2.4	0.4	On-board address latch; reduced-power standby mode
DIP, SOJ, LCC	1.2	350 mW (max)	2.2	0.8	2.4	0.4	2V data retention
DIP, SOJ, LCC, ZIP	1.2	350 mW (max)	2.2	0.8	2.4	0.4	2V data retention
DIP, SOJ	0.8	350 mW (max)	2.2	0.8	2.4	0.4	2V data retention
64-pin ZIP	N/A	1.32W (min)	2.2	0.8	2.2	0.4	On-board bypass capacitors for circuit protection
DIP	2.0	440 mW/121 mW	2.2	0.8	2.4	0.4	
DIP, SOJ	0.7	660 mW/165 mW	2.2	0.8	2.4	0.4	
DIP, SOJ	0.7	400 mW/5 mW	2.2	0.8	2.4	0.4	Configurable as ×1 or ×4
DIP, SOJ, TSOP	0.8	385 mW/0.27 mW	2.2	0.8	2.4	0.4	Thin small-outline packaging
DIP, SOJ	1.0	800 mW (max)	2.2	0.8	2.4	0.4	Non-address-transition detection design
52-pin PLCC	1.2	1.0W (typ)	2.2	0.8	2.4	0.4	On-board MUX for use with DSP6001
52-pin PLCC	1.0	1.0 to 1.5W (typ)	2.2	0.8	2.4	0.4	Suitable for use with 33-MHz R3000 μPs
24-pin DIP, flatpack	1.1	960 mW (max)	–1.165	–1.475	–1.025	–1.62	Balanced read/write cycle times; >200-mA latch-up immunity
28-pin DIP, flatpack	1.1	1.365W (max)	–1.165	–1.475	–1.025	–1.62	Balanced read/write cycle times; >200-mA latch-up immunity
28-pin DIP, flatpack	1.1	1.310W (max)	–1.045	–1.490	–0.900	–1.665	Balanced read/write cycle times; >200-mA latch-up immunity
28-pin DIP, SOJ, LCC	1.0	400 mW/100 μW (L version)	2.0	0.8	2.4	0.4	Separate data input and output pins
28-pin DIP, SOJ, LCC	1.0	400 mW/100 μW (L version)	2.0	0.8	2.4	0.4	
DIP, SOJ	1.2	660 mW (max)	2.2	0.8	2.4	0.4	On-board comparator for cache-tag
DIP, SOIC	1.2	300 mW (max)	3.0	0.8	2.4	0.4	2V data retention
28-pin DIP	1.2	300 mW (max)	2.2	0.8	2.4	0.4	Power-failure control circuit and 11-year battery
28-pin DIP, 32-pin LCC	0.8	1W (typ)	2.0	0.8	2.4	0.4	Mil spec; integrated nonvolatile EEPROM
52-pin PLCC	0.8	200 mW (typ)	2.2	0.8	2.4	0.4	Mode-control pin allows alternative organizations
32-pin DIP, SOIC	0.8	300 mW/50 μW	2.2	0.8	2.4	0.4	
DIP, LCC	1.0	632 mW (max)	2.2	0.8	2.4	0.4	Mil spec; 6-T memory cell
DIP, LCC	0.8	825 mW (max)	2.2	0.8	2.4	0.4	Mil spec; 6-T memory cell
28-pin DIP, SOJ	1.0	742.5 mW/0.11 mW	2.2	0.8	2.4	0.4	Output buffer control
32-pin 525-mil SOIC	1.0	385 mW (max)	2.4	0.8	2.4	0.4	Data retention in self-refresh mode
DIP, SOIC	1.5	200 mW/0.5 μW	2.2	0.8	2.4	0.4	Standby and low-power versions
DIP, SOJ	1.2	600 mW/500 μW	2.2	0.8	2.4	0.4	9-nsec output enable
52-pin PLCC	1.2	2W/1.3W	2.2	0.8	2.4	0.4	Direct interface with 82385 cache controller
22-pin DIP	0.8	<1W (typ)	2.1	0.8	2.4	0.5	Rad hard; fully static operation
DIP, LCC, PLCC	0.8	<1W (typ)	–1.1	–1.54	–1.02	–1.62	Rad hard; fully static operation
24-pin LCC, PLCC	0.8	400 mW (typ)	–1.4	–1.8	–1.3	–1.9	Rad hard; fully static operation; registered data I/O
DIP, SOJ, SOG	1.0	600 mW (max)	2.2	0.8	2.4	0.4	Mil spec; 6-nsec chip-select to output valid
52-pin PLCC	0.9	750 mW (max)	2.2	0.8	2.4	0.4	Direct interface with Intel's 80385 cache controller
28-pin SOJ	0.8	350 mW/100 μW	2.2	0.8	2.4	0.4	

Timing factors, trace routes, pc-board construction, line lengths, power distribution, and heat dissipation all affect your system's noise levels.

ance, depending on how you configure the system.

If you're working on a project that must meet military radiation-hardness specs, GaAs SRAMs from Vitesse may be your best choice. GaAs offers the fastest performance levels available and is inherently resistant to the effects of radiation. However, yields are low, and there aren't many parts to choose from. Vitesse's VS12G476 1k×4-bit SRAM boasts a 3-nsec read/write cycle time and dissipates less than 1W. The company attributes its chip's low power specs to a proprietary enhancement/depletion-mode-fabrication technology. The VS12G476's $64 price tag makes it quite a bargain when compared with Harris Semiconductor's CMOS rad-hard SRAM, which sells for $800 and has an access time of 90-nsec.


__If you want to add nonvolatility__ and a real-time clock to your system, you can simplify the task by integrating SGS-Thomson's Timekeeper RAM into your design.

In an effort to simplify the task of interfacing GaAs memories to any silicon-based components that may reside on the same board, Vitesse offers GaAs SRAMs that have TTL- and ECL-compatible I/O lev-

Manufacturers of Static RAMs

For more information on static RAMs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Advanced Micro Devices
Box 3453
Sunnyvale, CA 94088
(800) 538-8450;
in CA, (408) 732-2400
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els. And the company is actually shipping the parts—an important fact when you consider the number of GaAs manufacturers that offer a wide selection of vaporware.

Fortunately, increasing the amount of memory in your system is a much simpler design task than increasing the memory's speed. Pin compatibility is the key to increasing a system's memory simply. It lets you pop out your old 256k-bit chips and plug in 512k- or even 1M-bit replacements, such as Mitsubishi's 35-nsec 1M-bit CMOS TTL SRAM for $195 (100). When upgrading the size of your memory cache by using pin-compatible monolithic SRAMs, no unusual hardware-design constraints typically apply. When deciding which high-density SRAM you should purchase, ask if the manufacturer can scale its fabrication technology to higher densities for future products.

If you need more density than the latest monolithic chips offer, many manufacturers offer SRAMs packaged as modular arrays with as much as 4M bits of memory bonded to a single substrate with DIP or ZIP pinouts. Logic Devices Inc has a 4M-bit SRAM module with access times as fast as 25 nsec. The module comes in a 48-pin DIP, and prices start at $288.

You can also turn to pseudostatic RAMs (PSRAMs) for low-cost, high-density memories. PSRAMs use a dynamic-RAM (DRAM) cell structure (one transistor and one capacitor) and an on-chip refresh-control circuit, which eliminates the need for an external refresh clock. Accordingly, circuits using

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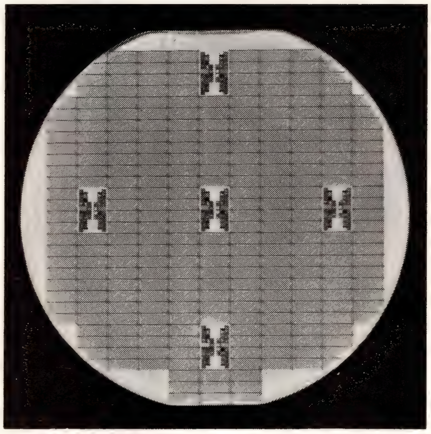

Using a proprietary 1M-bit CMOS process, *Paradigm Technology claims that its ICs have the smallest cell size among competitive 256k-bit SRAMs.*

PSRAMs are less complex and easier to implement than those using DRAMs. Motorola sells a 1M PSRAM called the MCM518128 with 80- or 100-nsec access times for $35 (500). Toshiba's November 1989 application note describes how to use its TS518129 1M-bit PSRAM.

If you have an embedded-processor application, Micron has an SRAM designed to meet your circuit's requirements. The MT5C1627 is a 2k × 8-bit SRAM with an on-chip address latch that eliminates the need for external address latches. This feature makes the chip well suited for multiplexed address/data bus applications by providing an interface that doesn't require glue logic. This 100-nsec part sells for $5 in sample quantities.

SRAMs are widely used as cache-tag memories. Logic Devices Inc and SGS-Thomson developed SRAMs that specifically suit this application by optimizing the memories' architecture with an on-chip address comparator. Logic's cache-tag devices come in speeds as fast as 10 nsec and have as much as 64k bits of storage. Prices start at $49.50. SGS-Thomson's 32-bit MK4202 sells for as little as $15.23 (1000) and has access times as low as 20 nsec.

If nonvolatility is critical in your application, Simtek, SGS-Thomson, and Dallas Semiconductor have battery-backed SRAMs that will protect your data. Dallas Semiconductor has a 1M-bit nonvolatile chip that has 100- and 120-nsec access times and a price tag of $95. Simtek has 64k-bit Mil-spec versions available with access times as short as 35 nsec and prices as low as $28.77. Both Dallas Semiconductor and SGS-Thomson have nonvolatile RAMs that contain real-time clocks. Dallas Semiconductor's 256k-bit DS1244 sells for $35 (100). SGS-Thomson's $9.40 MK48T87 plugs into the socket that contains the MC146818 real-time clock IC, which you'll find in every IBM PC. **EDN**

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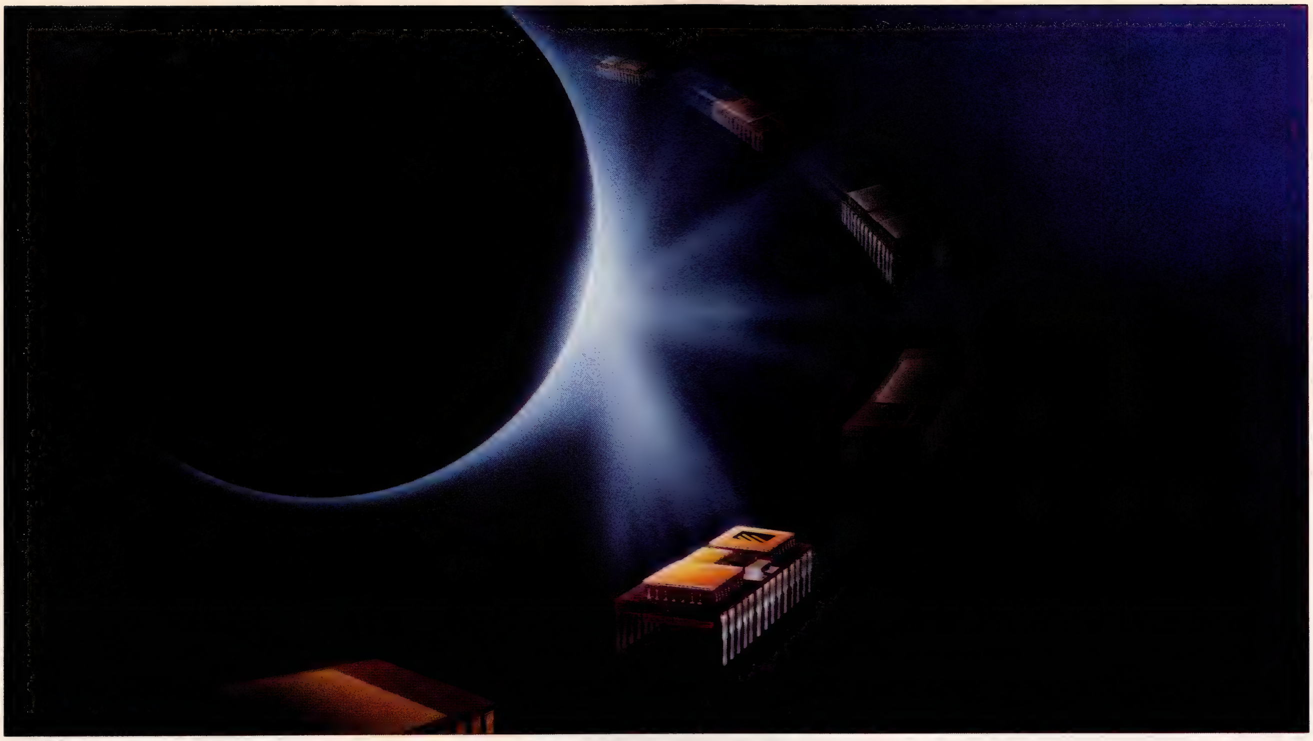

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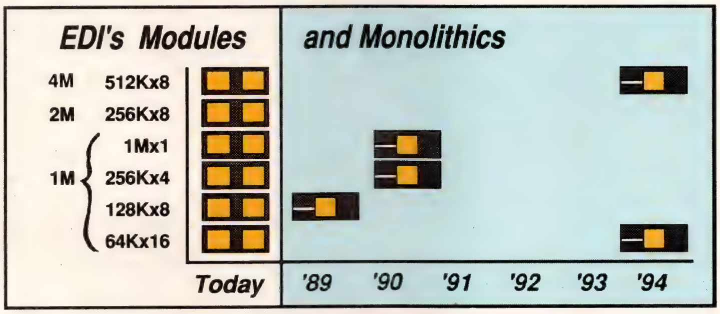

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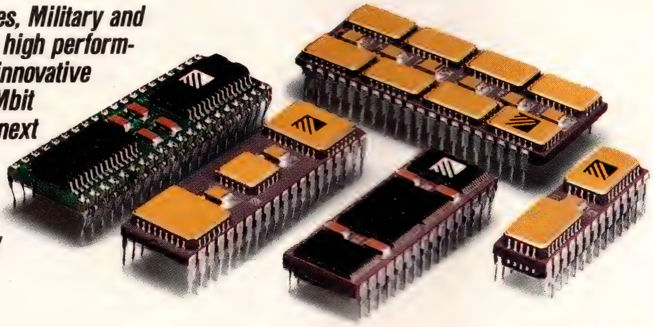

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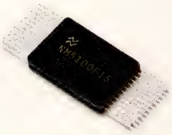
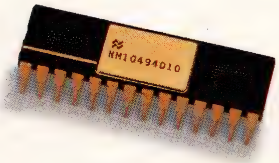


The original BiCMOS 256Kx1 at 15 ns

The new BiCMOS 64Kx4 at 12 ns



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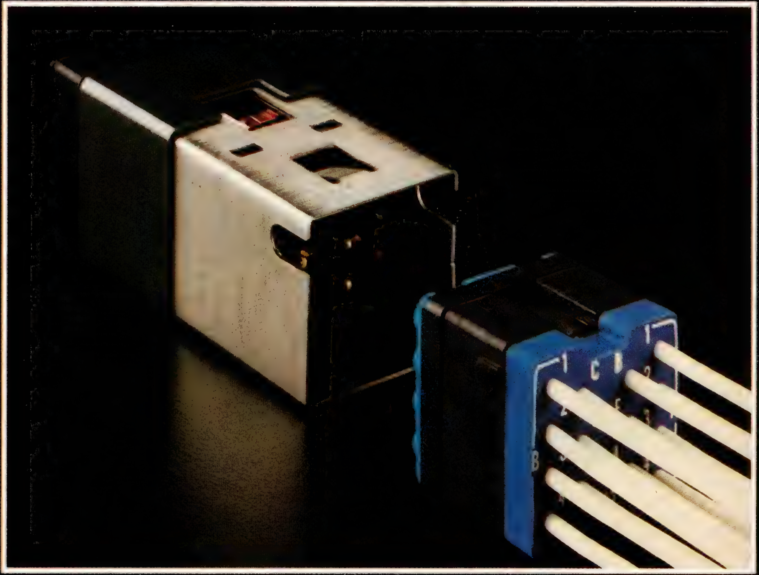

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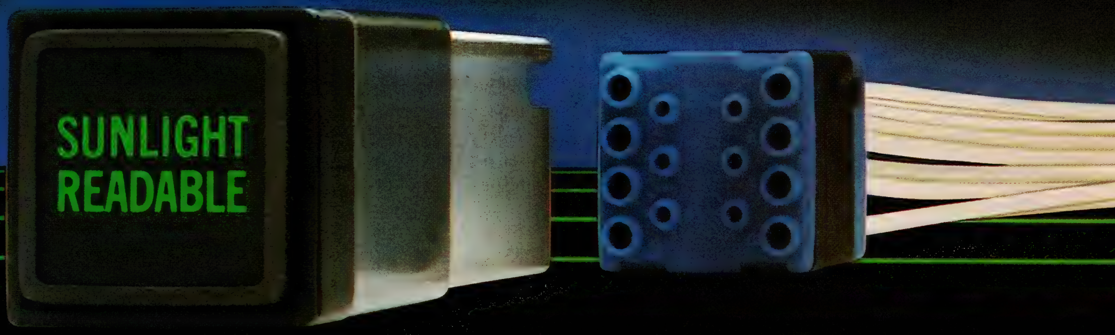

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DESIGNER'S GUIDE

Spice-compatible op-amp macromodels

Part 1

New Spice compatible op-amp model boosts ac simulation accuracy

Part 1 of this 2-part article shows how the existing macromodels of op amps are inadequate for simulation of today's fast devices and describes a new approach that yields improved ac- and transient-simulation accuracy. The focus is on the macromodel structure and on calculations of the necessary parameters. Part 2 will describe the implementation of this approach for modeling two recent op amps.

Mark Alexander and Derek F Bowers,
Precision Monolithics Inc

There is a definite trend towards a comprehensive circuit-simulation approach—we believe that 75% of all installed circuit simulators are being used for system, rather than IC, design. Almost all of these simulators are variants of Spice. With the growth of the electronics industry, system engineers have come to need increasingly accurate models for an ever larger number of integrated circuits, especially the ubiquitous operational amplifier. However, the increasing speed and complexity of these IC devices has caused problems that were never anticipated by the original developers of Spice.

Because of the large number of active devices in a typical op amp, circuit simulations that use only transistor-level models can take an unacceptable amount of time, particularly when the circuit contains several op amps. Even simple models of semiconductor devices consume a large amount of computing time, because of the multiplicity of nonlinear equations involved. In some cases, the time needed for a complete simulation might exceed the time necessary to build an engineering prototype. Obviously, such a situation would completely defeat the whole purpose of using Spice.

Fortunately, you can reduce simulation time by using a macromodel that represents the op amp as accurately as possible without using large numbers of transistors or other nonlinear devices. However, it is quite a challenge to design a macromodel that, for all intents and purposes, exactly mimics the real device. For an op-amp model to be of real use to the circuit designer, it must not only accommodate all important dc parameters, but also provide a reasonably close approximation of the ac characteristics over a region that extends well beyond the unity-gain crossover frequency.

Existing macromodels are inadequate

Macromodels for many op amps already exist in the device libraries of several available software simulators. Most of these models are based on the original work done by Graeme Boyle and his colleagues (**Ref 1**), who developed their macromodel during the mid-1970s to ease the CPU-time crunch on the already overloaded mainframe computers of the day. Boyle eliminated all but two transistors from his macromodel. The two remaining devices formed the differential-input stage of the op amp; all subsequent stages were

> *The Boyle op-amp macromodel has several deficiencies that prevent accurate simulation of today's fast and complex devices.*

implemented with linear controlled sources, passive components, and diodes. The transistors in the input stage were retained because they facilitated the simulation of real-world effects such as bias currents and variation of output dV/dt with the differential input voltage.

Because Boyle's method greatly reduces the number of overall nonlinear elements, the simulation time required per amplifier also decreases substantially. The Boyle structure is certainly an improvement over a full transistor-level simulation, but the structure still has several deficiencies, which prompted the development of the new macromodel. The deficiencies are as follows:

- The Boyle model provides only two poles (and no zeros) for shaping the frequency-response of the complete amplifier—a configuration that is barely adequate for slower op amps, and completely insufficient for today's faster devices.
- All internally generated node voltages are referenced to ground, even if the amplifier is "floated" with respect to ground. This configuration is not representative of the true operation of an op amp—almost none of the available devices provide a ground reference.
- The output-terminal current flows out of a controlled source connected to ground, instead of from the power-supply rails as it would in a real amplifier. This feature completely precludes the simulation of circuits that depend on the amp's output current splitting correctly between the supply rails.

Ideal elements can reduce complexity

The circuit topology of the original Boyle model (**Fig 1**), was developed using two basic macromodeling techniques (called simplification and build-up) that proved very useful in the development of the new macromodel as well.

The simplification technique successively reduces the complexity of major internal stages of the op amp by using simple ideal elements to replace real portions of the circuit. Therefore, you can expect a functional block that uses this approach to closely resemble the actual circuit. In **Fig 1**, the model of the input stage is a good example of simplification. The model retains the differential-input characteristics of an emitter-coupled pair, but eliminates any active loads; it replaces the tail-current source with an ideal element; and it assumes the task of generating the second amplifier pole. Adding a single capacitor (C_E) allows the model to provide a pole in this stage, and the reduction in overall

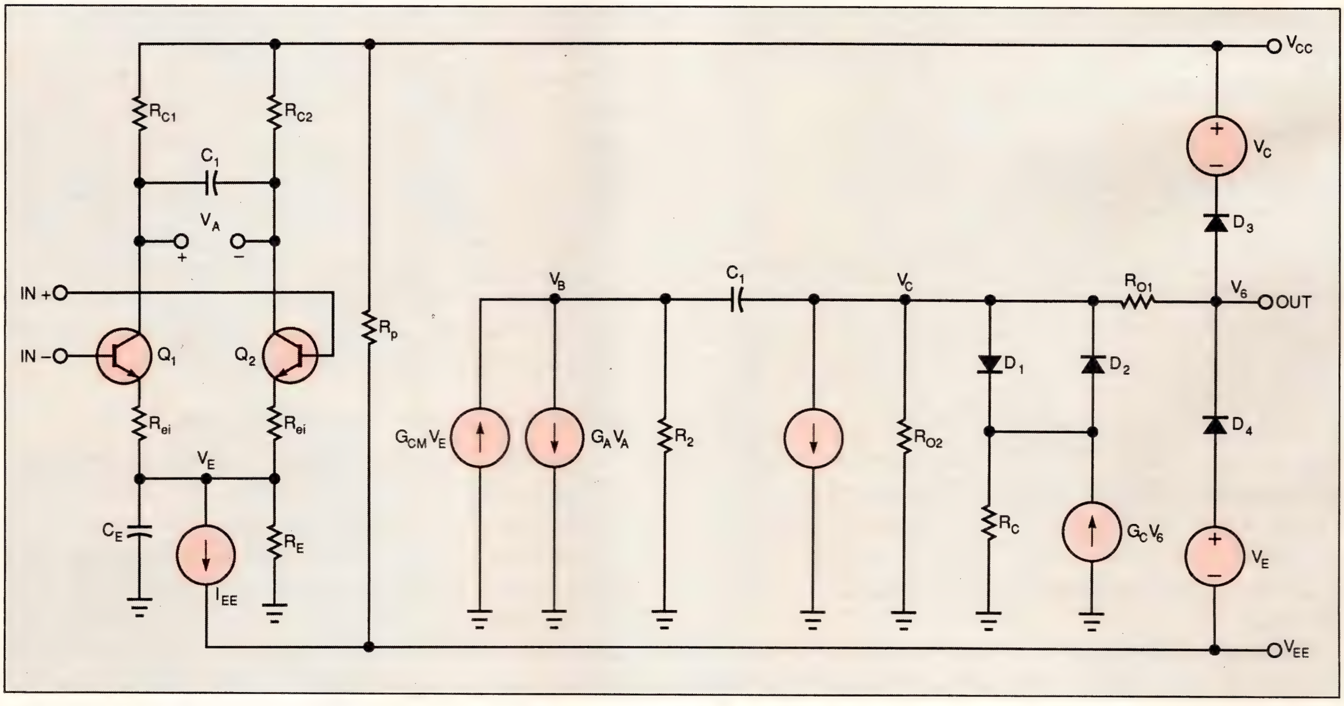

Fig 1—A serious disadvantage to the Boyle op-amp macromodel *is that all voltages are referenced to ground.*

component count makes the simulation run faster.

The build-up technique, on the other hand, lets you construct a circuit block composed entirely of ideal elements, which very closely emulates the behavior of the real section of the device. Unfortunately, the build-up technique often results in subsections that bear little resemblance to their physical equivalents. **Fig 1**'s output stage is a good example: it provides the necessary output voltage clipping, has the correct output resistance, and also provides short-circuit current limiting, but does not look like anything one would expect to find in the schematic of a real op amp.

Development of an improved macromodel

The impetus behind the new macromodel (**Fig 2**), arose out of the desire to create a model that operates like a real op amp. Yet it still had to be simple enough so that it would suffice as a generic model. **Figs 3**, **4**, and **5** show that the model consists of several cascaded sections that process the input signal.

The input stage is very similar to the Boyle model's because the simplification technique was used in its construction. However, after the input stage all similarity between the two macromodels disappears because of the way the build-up method was used to generate the rest of the new model. Notice that there is no ground reference in any of the signal-processing blocks. Instead, after differential to single-ended conversion, all internally generated node voltages are referred to the midpoint between the supply rails. This midpoint, called V_H in the model, is generated by two equal resistors connected between the supply rails.

The minimum requirement for modeling any particular op amp with the new macromodel is essentially the same as for the Boyle topology: a differential-input stage, a gain stage, and an output stage. This configuration yields a basic two-pole frequency response and allows direct comparisons between the two types of macromodels in terms of simulation time. You can add any combination of unity-gain pole, pole-zero, and zero-pole blocks between the gain stage and the output stage in order to obtain the desired frequency-dependent roll-off of the open-loop gain. The difference between the blocks is that the pole-zero block generates a pole at a lower frequency than that of the zero, whereas the zero-pole block generates a pole at a higher frequency than that of the zero.

Box 2, "Calculation of model parameters," shows the calculations that you must perform in order to construct an op-amp model based on the building blocks of **Figs 3**, **4**, and **5**. You can do these calculations quite easily on a hand calculator, given certain data-sheet

Text continued on pg 148

The evolution of Spice simulators

The electrical-circuit simulator Spice, and the more powerful version called Spice2, originally emanated from the University of California, Berkeley, during the 1970s (**Ref 4**). Primarily written for the purpose of assisting design engineers with the analysis of integrated circuits at the transistor level (hence the acronym *S*imulation *P*rogram with *I*ntegrated *C*ircuit *E*mphasis), Spice lets you use a computer to evaluate your designs more quickly and more thoroughly than is possible by means of laborious hand calculations. The popularity of Spice soon spread to the system-level-design community for the same reasons that the IC designers embraced it.

The original version of Spice was a public-domain program available at a purely nominal charge; however, many software vendors have recognized the need for a fully supported, adapted, and improved commercial circuit simulator. The first mainframe-based versions of such programs included HSpice from Meta-Software, I-Spice from NCSS timesharing, and PRECISE from Electronic Engineering Software. Recently, most mainframe versions have been adapted for use on workstations, and some have been adapted for IBM PCs and compatibles.

The first PC-based version of Spice was PSpice from MicroSim Corp. It was followed by others, such as IS-Spice from Intusoft. Other companies, including Analogy Inc (which offers a behavioral-simulation package known as Saber), have chosen to depart from the conventional Spice format of using "boxed" circuit elements to construct models. Instead, Saber relies on rigorous defining equations written in a specific modeling language, called Mast, to control the behavior of any desired electrical circuit model.

Calculation of model parameters

The following equations allow you to create an improved macromodel for simulation of any op amp. The calculations are given separately for each of the available building blocks, and some power-supply considerations are discussed.

Input- and gain-stage calculations

a. General calculations

Refer to **Fig 3** to identify components and signals mentioned here. First, choose I_{EE} such that it is somewhat less than the amp's total quiescent current. For convenience, you may set I_{EE} to 1 mA, 100 μA, 10 μA, or 1 μA. Then,

$$C_2 = C_3 = \frac{I_{EE}}{\text{SLEW RATE}}$$

$$R_7 = R_8 = \frac{1}{2\pi\, f_{p1}\, C_2},$$

where f_{p1} = dominant amplifier pole.

$$G_1 = G_2 = \frac{A_{VOL}}{R_7},$$

where A_{VOL} = open-loop dc gain

$$R_3 = R_4 = \frac{1}{G_1}$$

$$C_1 = \frac{1}{4\pi\, f_{p2}\, R_3},$$

where f_{p2} = second amplifier pole

$$V_1 = V_{CC} - (+V_{OUT\,MAX}) + V_T \ln(2I_{EE}/I_S)$$
$$V_2 = (-V_{OUT\,MAX}) - V_{EE} + V_T \ln(2I_{EE}/I_S)$$
$$V_T = 0.02585\text{V AT } T = 27^\circ\text{C}$$
$$I_S = 1\times10^{-12}\text{ A (FOR BOTH DIODES).}$$

You can substitute some data-sheet parameters directly into the model. These parameters are: E_{OS} = input offset voltage (dc component only); I_{OS} × input offset current; C_{IN} = input capacitance.

b. Bipolar input-stage calculations

First, you must evaluate the following equation to determine whether the op amp in question can be modeled using the new macromodel:

$$A_{VOL} \le \frac{\text{SLEW RATE}}{4\pi\, f_{p1}\, V_T},$$

where V_T = 0.02585V at 27°C.

If the equation holds true, then you may proceed with the rest of the calculations. If not, then you must modify the model to accommodate this particular op amp. Part 2 of this article will discuss the modifications and will give an example of how to modify the model for a real op amp that does not meet the above criterion.

$$R_5 = R_6 = R_3 - \frac{2\,V_T}{I_{EE}}$$

$$\beta_F = \frac{2\,I_{BIAS}}{I_{EE}},$$

where β_F is the forward current gain of the input transistors, and I_{BIAS} is the input bias current.

$$R_1 = R_2 = \frac{1}{2\left(\frac{1}{R_{ID}} - \frac{1}{2\,\beta_F\, R_3}\right)} \le 5\times10^{11}\ \Omega,$$

where R_{ID} is the differential input resistance. If R_{ID} is not a specified data-sheet parameter, then set both R_1 and R_2 to the value $5\times10^{11}\Omega$.

c. JFET input-stage calculations

If your design has a JFET input stage, use the default value of −2.000V for the gate-to-source cutoff voltage V_{TO}. Also, change the name of the first-stage current source to I_{SS}. The main calculation is to determine β, the JFET gain factor:

$$\beta = \frac{(G_{½})^2}{2\,I_{SS}},$$

where I_{SS} is the first-stage tail current.

For maximum output dV/dt, the tail current must originate from one side only of the differential pair; this condition requires a differential input voltage equal to:

$$V_{ID}=\frac{\sqrt{2}\ (\text{SLEW RATE})}{2\pi\ A_{VOL}\ f_{p1}}$$

Also, the input bias current is composed of the gate-drain and gate-source leakage currents. Thus,

$$I_S=\frac{I_{BIAS}}{2},$$

where I_{BIAS} is the input bias current at 27°C. Further,

$$R_1=R_2=\frac{R_{ID}}{2},$$

where R_{ID} is the differential input resistance (normally $1\times10^{12}\Omega$.

Finally, you can set the values of R_5 and R_6 to zero, because degeneration is not normally needed with JFET input amplifiers.

Frequency-shaping-stage calculations

To identify parameters of the frequency-shaping stages, refer to **Fig 4.** In all three types of the frequency-shaping stage, set G_3 and G_4 to $I\times10^{-6}$ times A/V, for convenience. Further, f_Z is the zero frequency and f_P is the pole frequency.

Then for the pole-zero stage,

$$R_{11}=R_{14}=1\times10^6$$
$$R_{12}=R_{13}=\frac{R_{11}}{f_z/f_p-1};$$
$$C_4=C_5=\frac{1}{2\pi\ f_z\ R_{12}}$$

for the zero-pole stage,

$$R_{16}=R_{17}=1\times10^6$$
$$R_{15}=R_{18}=(f_p/S_z-1)\ R_{16};$$
$$L_1=L_2=\frac{R15/16}{2\pi\ f_p}$$

for the pole stage,

$$R_{21}=R_{22}=1\times10^6$$
$$C_6=C_7=\frac{1}{2\pi\ f_p\ R_{21}}.$$

Common-mode-gain-stage calculations

To identify the parameters of the common-mode gain stage, refer to **Fig 4.**

$$R_{19}=R_{20}=1\times10^6$$
$$G_7=G_8=\frac{1}{R_{19}\times\text{CMRR}},$$
$$L_1=L_2=\frac{R_{19}}{2\pi\ f_{p(CM)}}$$

where f_{CM} is the common-mode pole.

Output-stage calculations

To identify the parameters of the output stage, refer to **Fig 5.** The breakdown voltage of diodes D_7 and D_8 is nominally set to 50V. The value of inductor L_3 is determined by experiment. R_{OUT} is the open-loop output resistance; V_T is 0.02585V at 27°C; and I_S is 1×10^{-12}A for all diodes. Then,

$$G_{11}=G_{12}=G_{13}=G_{14}=\frac{1}{2\ R_{OUT}}$$
$$R_{23}=R_{24}=2\times R_{OUT}$$
$$V_3=I_{SC}(+VE)R_{OUT}-V_T\ln(20\times10^{-6}/I_S)$$
$$V_4=|I_{SC}(-VE)R_{OUT}|-V_T\ln(20\times10^{-6}/I_S).$$

You can determine the values of resistors R_9 and R_{10} in **Fig 3** by means of the following equation:

$$R_9=R_{10}=\frac{1}{2(dI_{SY}/dV_{SY})},$$

where dI_{SY}/dV_{SY} represents the variation of supply current caused by a change in the supply voltage. The total quiescent current that flows between V_{CC} and V_{EE} in the model is thus:

$$I_{SY}=I_{EE}+(N+1)\left(\frac{V_{CC}-V_{EE}}{2R}\right)+I_{DC}+\left(\frac{V_{CC}-V_{EE}}{R_9+R_{10}}\right),$$

where N is the total number of frequency-shaping and common-mode gain stages in the model;
R is normally $1\times10^6\Omega$; this value, along with the transconductance of the G-sources in the frequency shaping stages, can be appropriately scaled for low-power op amps;
and I_{DC} is the dc offset added to the G_1 and G_2 sources to make up the difference between the current drawn by the rest of the model and the quiescent current of the actual amplifier (I_{SY}).

The modular structure of the new macromodel lets you simulate op amps with any number of poles and zeros that may be needed for waveshaping.

parameters of the op amp in question, together with the necessary pole/zero locations.

The input stage (**Fig 3**) is a simplified 2-transistor circuit. One major difference between the new model and its predecessor is that, in the new model, the input stage uses the same type of input devices as the physical op amp—that is, npn or pnp bipolars, p-channel JFETs (or n-channel devices where applicable), or MOSFETs. The Boyle model allows *only* for bipolar devices in its input stage, which are fine if a bipolar input op amp is being modeled. However, when you model a FET input op amp with the Boyle technique, you have to dramatically increase the current gain of the input transistors in order to obtain the desired input bias current. You must also use emitter degeneration to reduce their transconductance. The result of these modifications is that the usual variation of output dV/dt of a FET input amplifier over a fairly wide input-differential voltage range (typically 1 to 2V) will not be correctly simulated. A degenerated bipolar input stage has a linearized, hyperbolic-tangent transfer characteristic (**Ref 2**), whereas a FET input stage has a square-law transfer characteristic (**Ref 3**). Obviously, these characteristics are not equivalent. Therefore, because the parameter calculations for a FET input stage are no more complicated than those for a bipolar stage, it makes sense to use the correct input devices in the model.

All input-stage parameters (such as offset voltage, offset current, and input capacitance) that exhibit nonideal behavior are modeled using separate ideal elements. Also, two equal resistors are connected between the inverting and noninverting input terminals to generate the common-mode input voltage. The input voltage is used in a later section of the model, where it is scaled and frequency-shaped before being fed back

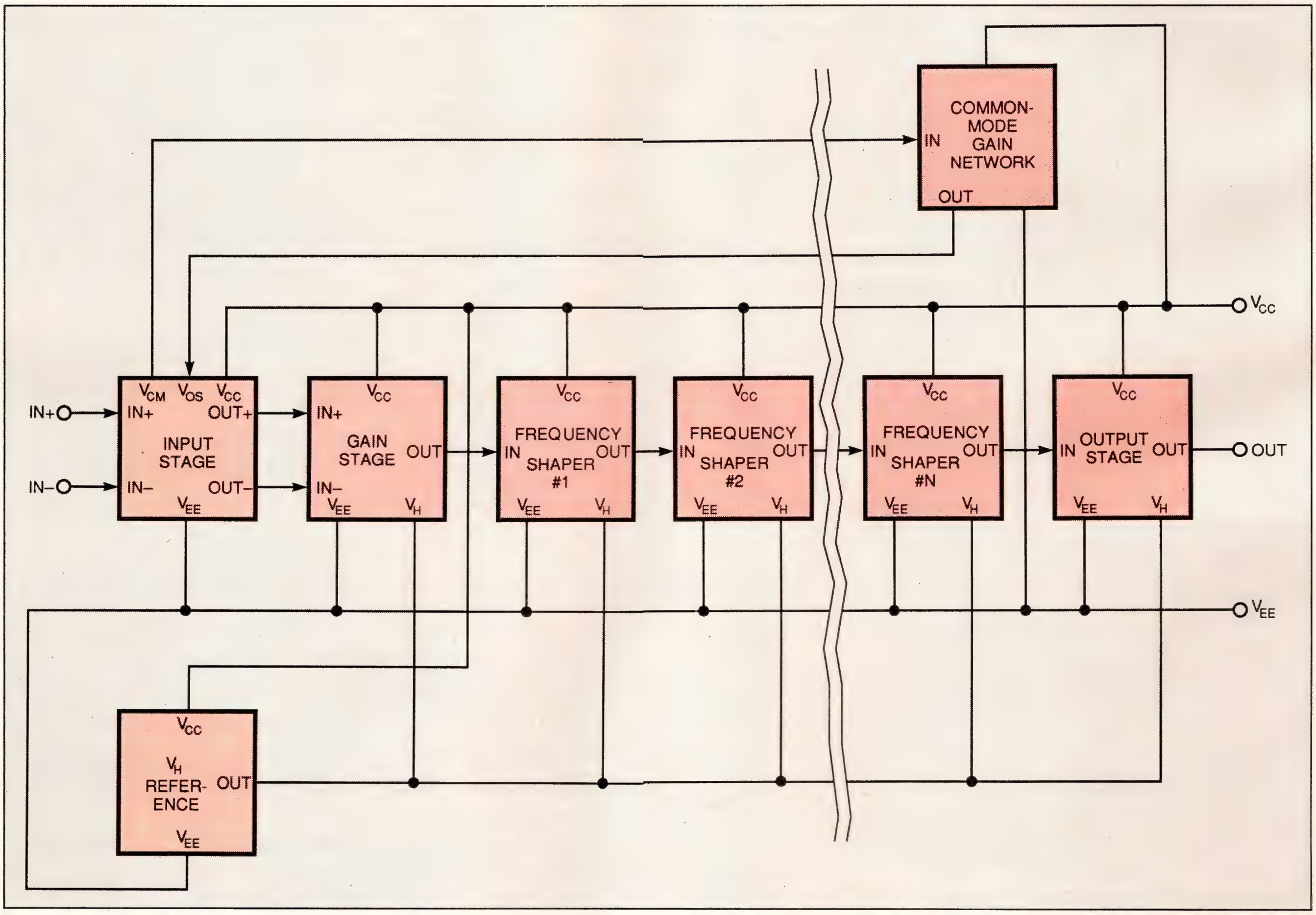

Fig 2—The new op-amp macromodel is inherently modular. *You can cascade any of the building blocks to obtain any number of poles and zeros in your op-amp design.*

into the input stage as a modifier to the offset voltage.

The model assumes that the input transistors are perfectly matched and do not have any junction capacitance that would alter the overall frequency response. It does account for the correct input-bias current, however, through appropriate choice of current gain for the bipolar stage or gate-leakage currents for the FET stage. You set the voltage gain of the differential pair to unity by making the load resistor value equal to the reciprocal of the transconductance of the transistors. This assumption simplifies the calculations to determine the slew-rate-limiting components. Tail current for the input stage is nominally set to 1 mA for convenience; however, it can be scaled down to 100 μA, 10 μA, or 1 μA, depending on the amp's total quiescent current.

Gain stage features

The model's open-loop gain is normally achieved in a single stage (**Fig 3**), which consists of two voltage-controlled current sources, two resistors, two capacitors, and a voltage-limiting network. The conversion of signals from differential to single-ended form also takes place during this stage. The voltage-limiting network consists of a pair of diodes, each connected to its own voltage source. The network prevents the gain stage and the other internal nodes of the model from swinging beyond the power-supply-rail voltages during an input-overdrive condition. Voltage limiting *must* take place in the open-loop gain stage; otherwise, succeeding nodes could attempt to simulate the generation of huge (hundreds of kilovolts) signals.

Two capacitors, connected in parallel with the resistors, determine both the dominant amplifier pole and the slew rate. At present, the macromodel can handle only symmetrical positive and negative slew rates, because symmetry is the easiest condition to simulate. However, future enhancements may allow for some variation between them. Finally, to each of the two voltage-controlled current sources, the stage adds a dc component that makes up the bulk of the amp's quiescent supply current.

Investigation of op-amp frequency response reveals that, in most cases, accurate simulation of the gain and phase variation of real devices at high frequencies requires more than two poles. Further, different types of op amps have varying numbers of poles and zeros. To allow each of these diverse types to be easily con-

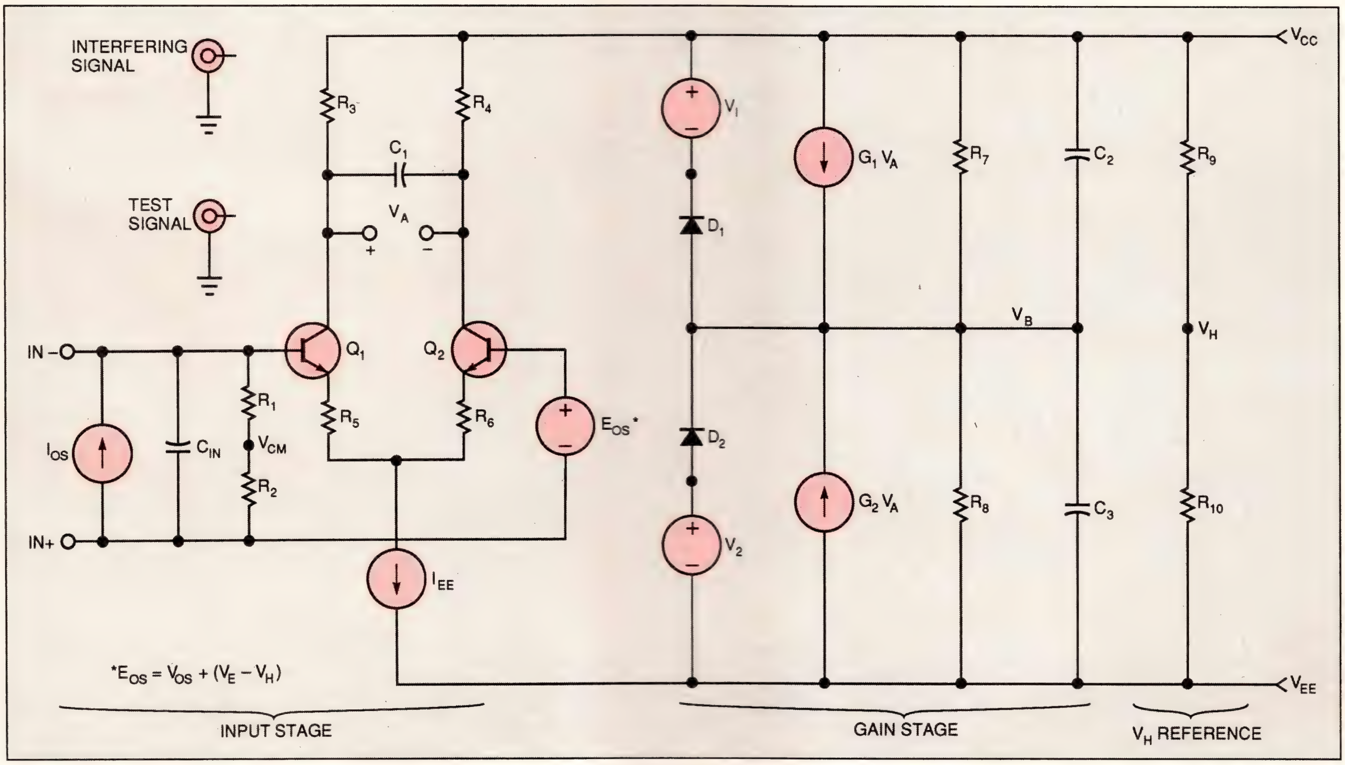

Fig 3—The input stage of the new model resembles that of the Boyle model, *but all succeeding stages have a radically different structure.*

All of the open-loop gain is supplied by one gain stage, which immediately follows the input stage and performs current limiting.

verted to a Spice-compatible subcircuit—without having to start from scratch every time—a truly general model would have to be highly modular and permit arbitrarily large numbers of poles and zeros. Therefore, the final structure uses a few basic building blocks that are common to all individual op-amp models; these blocks are shown in **Fig 4.**

All of the frequency-shaping blocks have unity gain at dc, because the g_m of each voltage-controlled current source (VCCS) is equal to the reciprocal of the resistance connected from each node of the VCVS (voltage-controlled voltage source) to the power-supply rails. This topology is advantageous because during model generation for a specific amplifier, you can comment out separate poles or pole/zero pairs. You can then see their effect, individually, on the net frequency response of the amplifier, so that pole/zero tweaking becomes rather easy. Because all the frequency-shaping blocks have unity gain at dc, the procedure does not alter the model's dc open-loop gain.

The common-mode gain stage (**Fig 4**) consists of two VCCSs that drive two equal resistors; each resistor is connected in series with an inductor to one of the supply rails. The inductors simulate the typical fall-off of CMRR that most amplifiers exhibit as the input frequency increases. The input common-mode voltage, relative to the V_h node, controls the current sources. Each controlled source has a g_m equal to the reciprocal of the associated resistor value divided by the CMRR of the amplifier at dc.

Accordingly, the gain from the input common-mode network to the internal common-mode gain node is equal to the reciprocal of the amplifier's CMRR. (The term "gain" is a misnomer here, because the common-mode gain has a value that is much less than unity).

The inductors add a zero to the common-mode gain, which is the same as adding a pole to the CMRR. The common-mode voltage, after being scaled and appropriately frequency-shaped, is then added back to the input stage as dictated by theory. This step is done by making the offset-voltage source in the input stage a unity-gain voltage-controlled voltage source, which has a dc component equal to the amplifier's V_{os}.

The operation of the output stage (**Fig 5**) is not

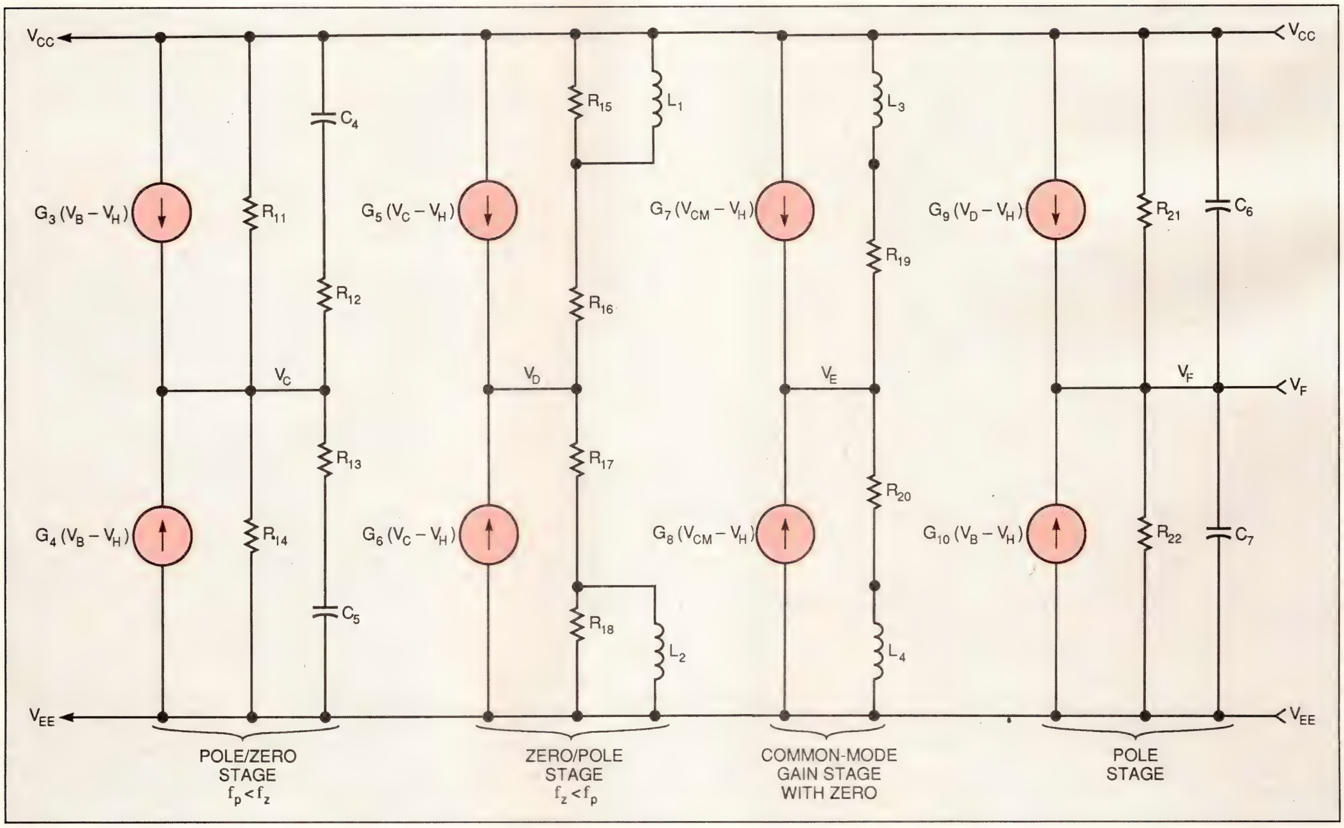

Fig 4—Three types of frequency-shaping networks are available, *in addition to a common-mode gain stage that provides a zero.*

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> *The unity gain of all waveshaping blocks lets you comment out individual blocks to determine their precise effect on the overall response of the op amp.*

entirely obvious. The internal op-amp output signal, after receiving all the appropriate frequency shaping, appears, at the last node prior to processing by the output stage, as a voltage referenced to V_h. The two voltage-controlled current sources in the output block drive two equal resistors connected to the supply rails, as with the other blocks. Here, however, the g_m of the two controlled sources is arranged so that they act as active current generators. Consequently, each g_m source generates just enough current to provide the desired voltage drop across its paralleled resistor.

When there is no load on the output, the model draws no current from either power-supply rail. It thus behaves somewhat like an ideal, unity-gain, class-B output stage with no crossover distortion. Because the two resistors are each equal to twice the open-loop output resistance, the output stage appears to act as a voltage source referenced to V_h with the correct dc output resistance. Simulating the right output resistance means that the dc open-loop gain will be properly reduced as the amplifier is loaded.

A subtle problem exists with this simple push-pull output stage, however. Regardless of whether the stage is sinking or sourcing current, the load current is always split equally between both rails—not exactly what a real output stage would do. So, with a sourced-load current, for example, the net positive supply current increases by only half the amount flowing in the load. The negative supply current decreases by the same amount. To compensate for this anomaly, you force a current from the positive rail to the negative rail exactly equal to half the load current. This correction current must always flow in the same direction—even if the output current reverses polarity.

The effect, therefore, of the two correction sources (**Fig 5**) is to force a unipolar compensating current between the power-supply rails that is equal to half the output current. In Spice, because there is no easy way to implement an absolute-value VCVS, there must be two linear correction sources—one for each half cycle of output current. The diodes in series with each source perform half-wave rectification, and the zeners ensure that there is always a conductive path for each source when its current reverses direction. The net result of all these additional elements is an output-stage model whose dc behavior very closely mimics that of the physical circuit.

To account for the typical rise in emitter-follower output-stage impedance with frequency, the macromodel includes an output inductor connected between the intermediate output node and the actual macromodel output node (**Fig 5**). You determine the value of this inductor, on a trial and error basis, by using capacitive loads on the model until the amount of over-

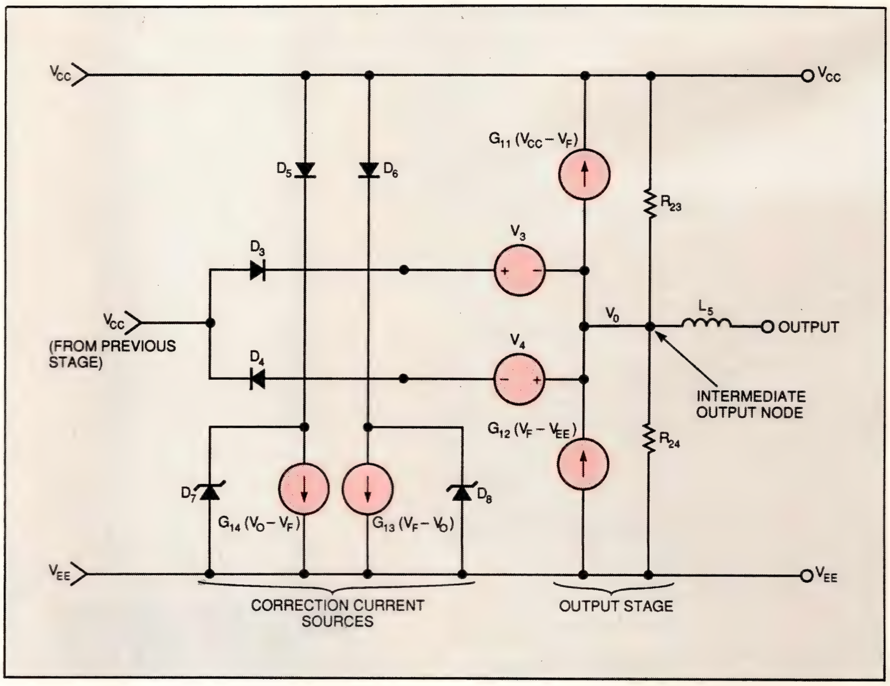
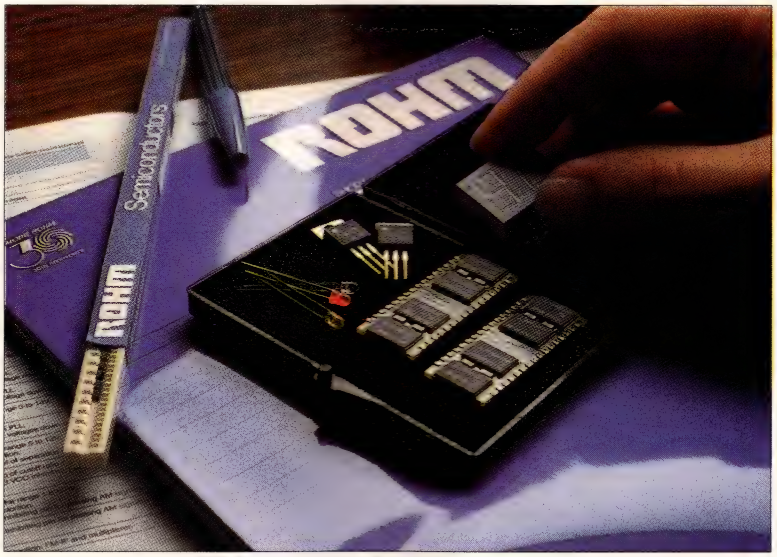


Fig 5—The new output stage is complemented by current sources, *which correctly split the load current between the power-supply rails.*

Real help.



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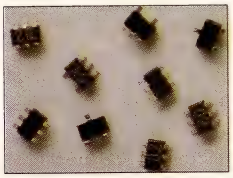

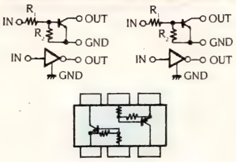

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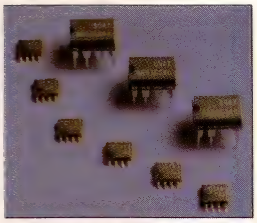

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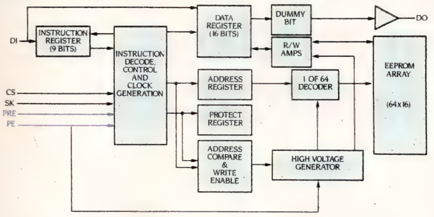

For more details, call Warren Schoals, the studious guy standing in the back. (Warren's also known as Mr. Whiteshirt when he's not out in his pick-up.)

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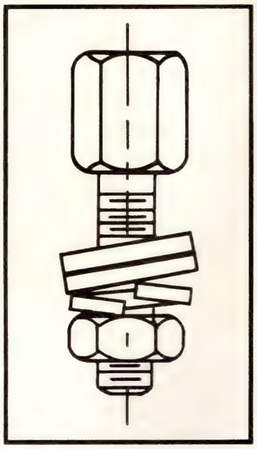

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shoot is very close to that which you observed with the real op amp and the same load.

Short-circuit current limiting is also a necessary feature of any good op-amp macromodel. In **Fig 5**, limiting is accomplished by clamping the output voltage (V_F) from the previous frequency-shaping stage to the intermediate output node (V_o), using diodes D_3 and D_4, and voltage sources V_3 and V_4. Remember that the signal from the previous stage is always equal to the ideal output voltage with no load, and that the output stage behaves as a voltage source with a finite output resistance. The action of the diodes and voltage sources is then equivalent to clamping the voltage drop across the effective output resistance. You can obtain the required output current limiting by an appropriate choice of each voltage source. **EDN**

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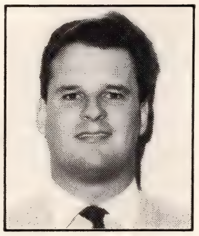
Authors' biographies

Derek F Bowers is staff vice-president of design at Precision Monolithics Inc, where he has worked for 11 years. He has been closely involved in the development of a wide variety of analog devices, including op amps, reference sources, and D/A and A/D converters. Derek holds a BSC in physics and mathematics from the University of Sheffield, England. In his spare time he enjoys music and brewing.



Mark Alexander has for nearly two years been a staff design engineer at Precision Monolithics Inc, where he is working on the design and development of digital-audio products that have not yet been announced. He holds a BASc (EE) from the University of Toronto, Canada. In his spare time he enjoys cooking, walking, and the design and construction of audio equipment. He is also a collector of antique watches.

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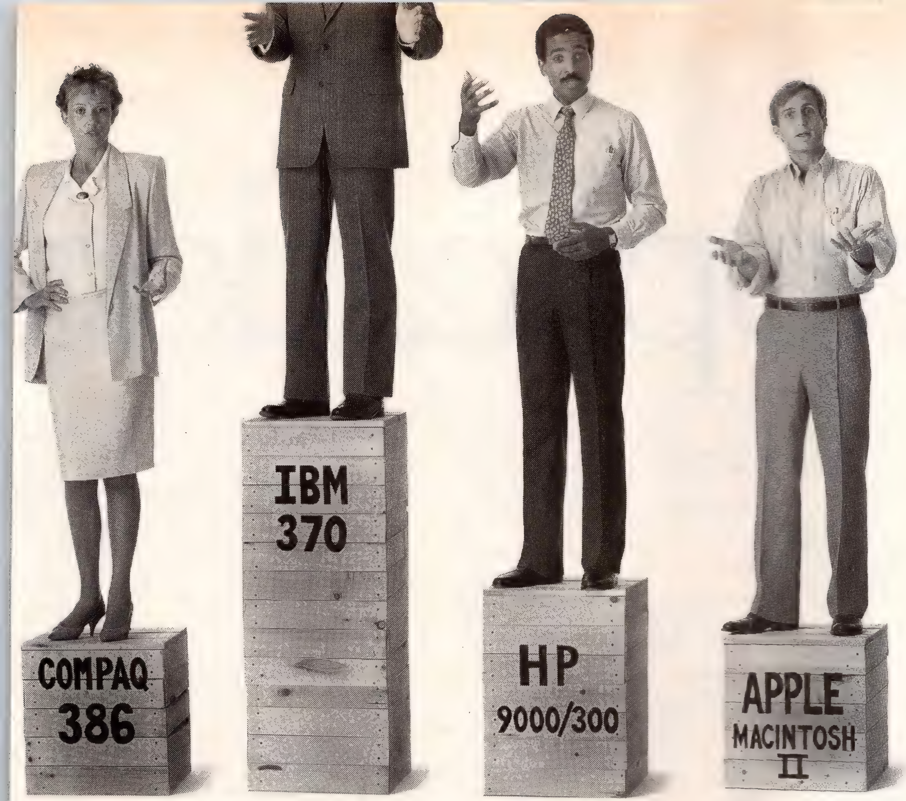

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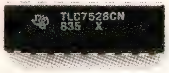

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CIRCLE NO. 102

Use a counter to characterize rapidly changing signals

You can greatly simplify characterizing dynamic and transient signals by using a universal counter that combines high precision and a fast measurement rate. Making dynamic measurements with a counter no longer requires that you construct a small system in which a desktop computer controls the counter and auxiliary instruments.

Lewis W Masters, *Guide Technology Inc*

In many respects a universal counter is analogous to a digital sampling oscilloscope (DSO). Both instruments can sequentially measure a parameter, be it time, frequency, or voltage, at reasonably precise intervals and store the results for display or analysis. The counter, of course, will characterize the dynamic variation of time intervals or frequency, rather than the dynamic variation of voltage. As with DSOs, a counter's resolution and sampling rate are key parameters. In both instruments, higher resolution and higher sampling rates open up significant new applications. Several universal counters are now available that deliver both sufficient precision and sufficient measurement speed to let you think of them as time-domain or frequency-domain "sampling scopes." In some situations, the "window" into circuit operation provided by a fast, high-resolution counter reveals even more than a DSO display can.

Most engineers believe that they need some type of frequency discriminator to characterize frequency-modulated (FM) signals, because neither an oscilloscope nor a spectrum analyzer will display detailed information about the modulating waveform. Many of these engineers will be surprised to learn that a frequency counter can *directly* demodulate an FM signal. In fact, when you link the counter to a computer with graphing capability, you can view the modulation waveform in near-real time. As with a DSO, the counter must acquire (sample) data at a rate sufficient to satisfy the Nyquist criterion for the modulating signal. For example, if a 200-Hz tone modulates a 75-MHz carrier, the counter must sample the signal much more often than 400 times/sec. A counter that samples at this rate allows you to visualize the modulation waveform and determine precisely the most important modulation parameters, such as peak deviation and symmetry, either from the display or by analyzing the original data. One significant advantage of this technique is its extraordinary dynamic range: a single data set can accommodate a step frequency change of more than 1000:1 while maintaining 1-ppm resolution.

You need a very special kind of counter

Most of the time- and frequency-measurement applications discussed in this article require you to make at least 1000 measurements/sec. Moreover, they demand a time-measurement resolution of at least 100

When you use a counter to demodulate a signal, it must acquire (sample) data at a rate sufficient to satisfy the Nyquist criterion for the modulating signal.

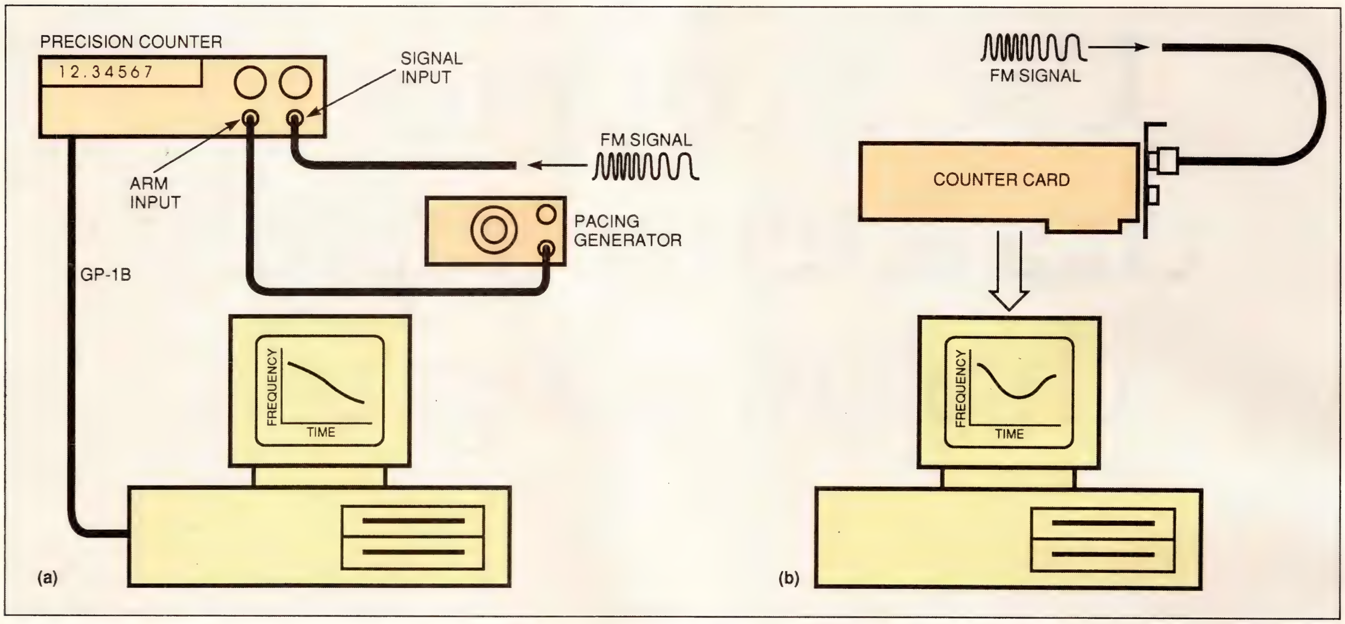


Fig 1—To perform frequency-domain sampling using a conventional precision counter (a), *you need both a pacing generator and an IEEE-488 controller (in this case a PC). A PC-resident counter/timer card* ***(b)*** *considerably simplifies the setup.*

psec. This fast data-acquisition rate precludes using the most common technique for achieving high resolution—time-interval averaging. The need to acquire 1000 very precise samples/sec mandates using a counter with exceptional capabilities: the instrument must resolve 10 digits in a 1-sec measurement. A counter with this resolution figure of merit can resolve a 1-ppm frequency deviation with a 1-msec gate time. Resolution and measurement speed are the most critical parameters for most applications. However, other features, such as internal measurement pacing and automatic graphing of results, are also important. A counter that integrates all these desirable features will save considerable setup and debugging time.

A universal counter can perform frequency-domain sampling using either of the two test systems shown in **Fig 1**. **Fig 1a** details the equipment and connections needed if you use a benchtop counter. You need the pacing signal generator to tell the counter when to start a measurement. The generator begins measurements by arming the counter via the external arm input. You need the IEEE-488 controller to acquire the data and to plot or analyze the results. **Fig 1b** shows the required connections for a PC-based counter. Because this counter provides an internal pacing function, you need no external generator.

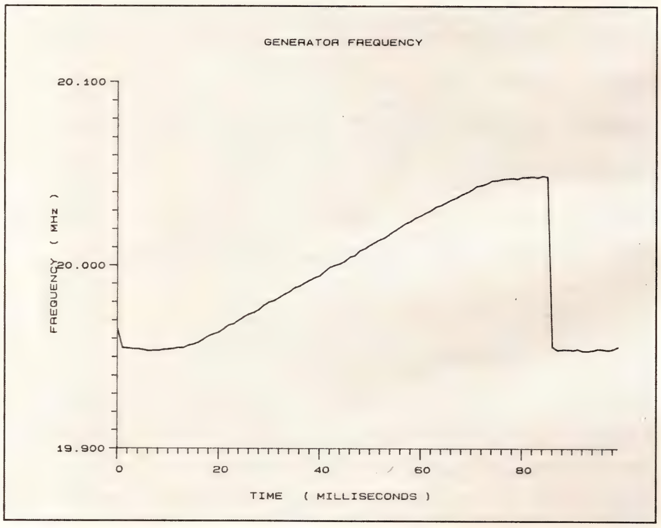


Fig 2—By making precise frequency measurements rapidly, *you can get a picture of how a sweep generator's output frequency varies with time. Note that this figure shows the generator's frequency—not the sweep voltage.*

Fig 2 shows a plot of an RF generator sweeping from 19.94 MHz to 20.07 MHz in 85 msec. This data, acquired in less than 0.1 sec, completely characterizes the sweep: It provides the linearity, the start frequency, the stop frequency, and the frequency slew rate. Furthermore, significant nonlinearities are immediately obvious. Note that this plot does *not* show the sweep voltage; it shows actual generator frequency vs time.

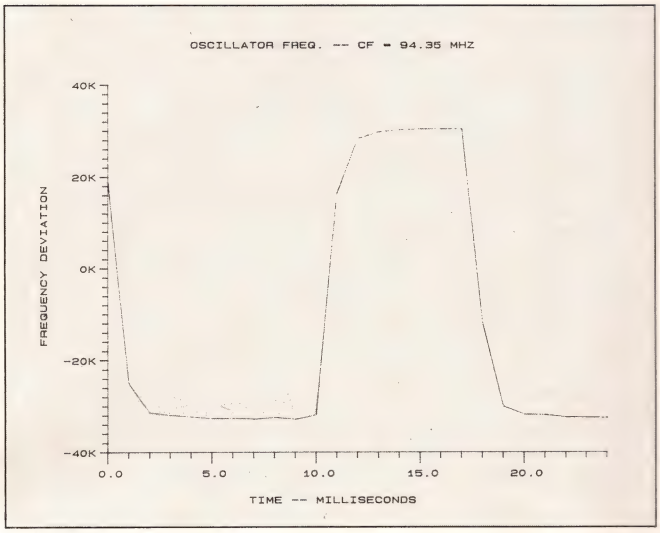


Fig 3—A fast, precise counter *can directly demodulate an FM carrier. Here, you see the modulating 50-Hz square wave recovered from a 94.35-MHz carrier. Note that you can directly observe the square wave's symmetry and its 60-kHz p-p frequency deviation.*

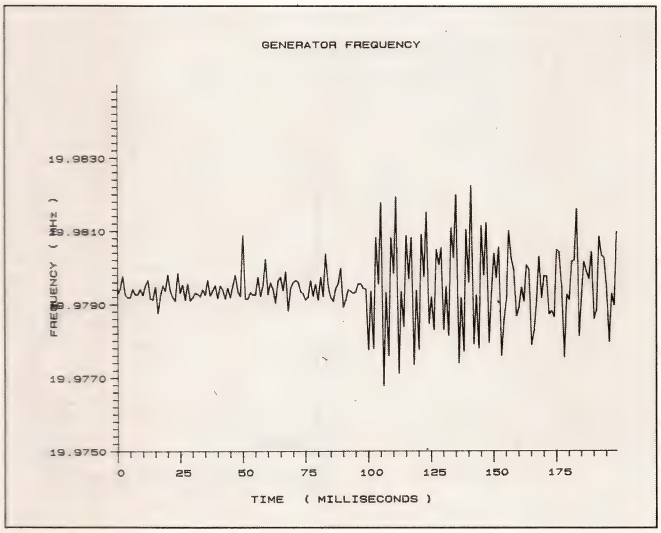


Fig 4—A counter can prove invaluable *in troubleshooting. Here it helps to pinpoint a stray field from a power supply's transformer as the cause of an oscillator's spurious modulation. The power supply—located close to the oscillator—was off for the first 100 msec.*

Note too that the start of this plot is synchronized to the initiation of the sweep. A feature called triggered pacing provides the synchronization by delaying data acquisition until the counter recognizes a trigger event. If the pacing were unsynchronized, the plot would inconveniently start at a random point on the sweep. Although most counters do not provide this feature, you can modify the setup of **Fig 1a** so that the sweep or modulation source triggers the pacing signal generator.

To most engineers, direct demodulation of an FM signal is a much more useful and common application than sweep-generator characterization. **Fig 3** shows the modulation information recovered by a counter directly sampling a 94.35-MHz carrier. Note that the modulating waveform, its frequency (60 Hz), the peak-to-peak deviation (60 kHz), and symmetry of the deviation are all clearly visible. The sample rate was 1000 samples/sec with a 0.25-msec gate time. With this setup, the counter can resolve frequency deviations as small as 500 Hz. Applications for direct demodulation abound in the design and analysis of RF circuits. For example, in most frequency bands, regulatory-agency rules limit an FM transmitter's peak deviation to prevent it from interfering with adjacent channels. A service or production facility could use a sampling counter to precisely measure the deviation. The same test could also verify that the modulation circuits were providing a linear and symmetrical FM signal.

RF and microwave engineers spend considerable effort tracking down sources of spurious modulation in oscillators, phase-locked loops, and frequency multipliers. Such diverse sources as microphonics from a cooling fan, ground loops on the pc card, or stray magnetic fields can generate interference. Although a spectrum analyzer is a very sensitive tool, it lacks one capability useful in troubleshooting: It cannot display the waveform of the offending interference. Furthermore, if the interference-driven frequency deviation is small, you'll need a costly, synthesized spectrum analyzer to see the problem at all. Conventional frequency counters are likewise powerless, because their long gate times simply average out the rapid frequency fluctuations, and their low measurement rates preclude sampling.

A high-resolution counter that is also capable of high measurement rates is an ideal instrument for RF troubleshooting. Even at 1000 samples/sec, the instrument can discern frequency deviations of nearly 1 ppm. **Fig 4** demonstrates the counter's ability to uncover spurious signals. The first half of the graph shows the frequency stability of a signal generator when it operates in the clockwise mode; the second half shows the incidental FM created when a laboratory power supply is near the generator. Clearly, the stray magnetic field from the power transformer induces a small but measurable amount of FM in the signal.

Designers of VCOs must often test the circuits for dynamic performance. That is, they must determine

The need to acquire 1000 samples/sec precludes using the most common technique for achieving 10-digit resolution—time-interval averaging.

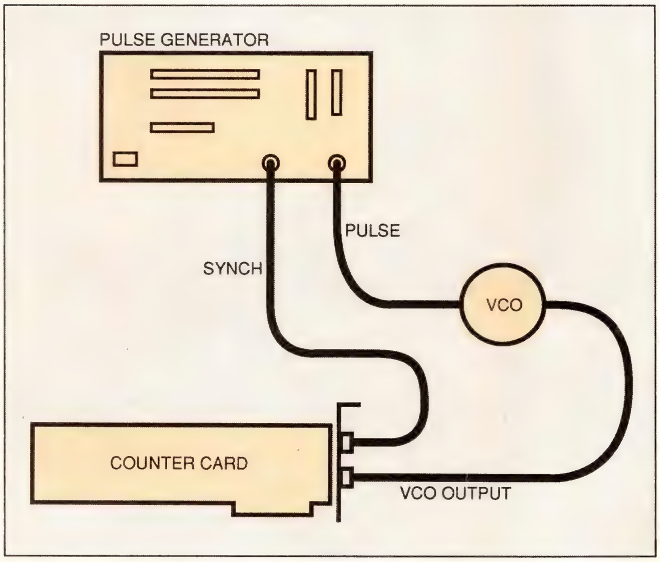


Fig 5—A pulse generator *is all you need to add to a high-performance counter to characterize the performance of a VCO in a single-shot measurement.*

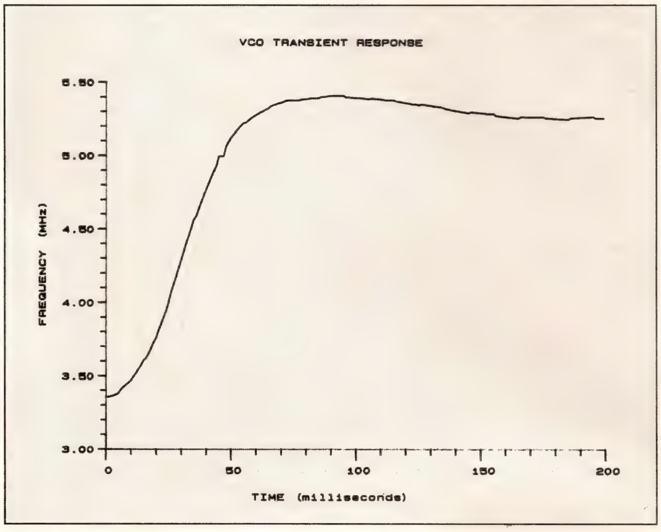


Fig 6—A picture of a VCO's response *to an input-voltage step not only shows the slew rate of the output frequency, but also indicates that the VCO briefly locked onto a 5-MHz oscillator located nearby on the pc board.*

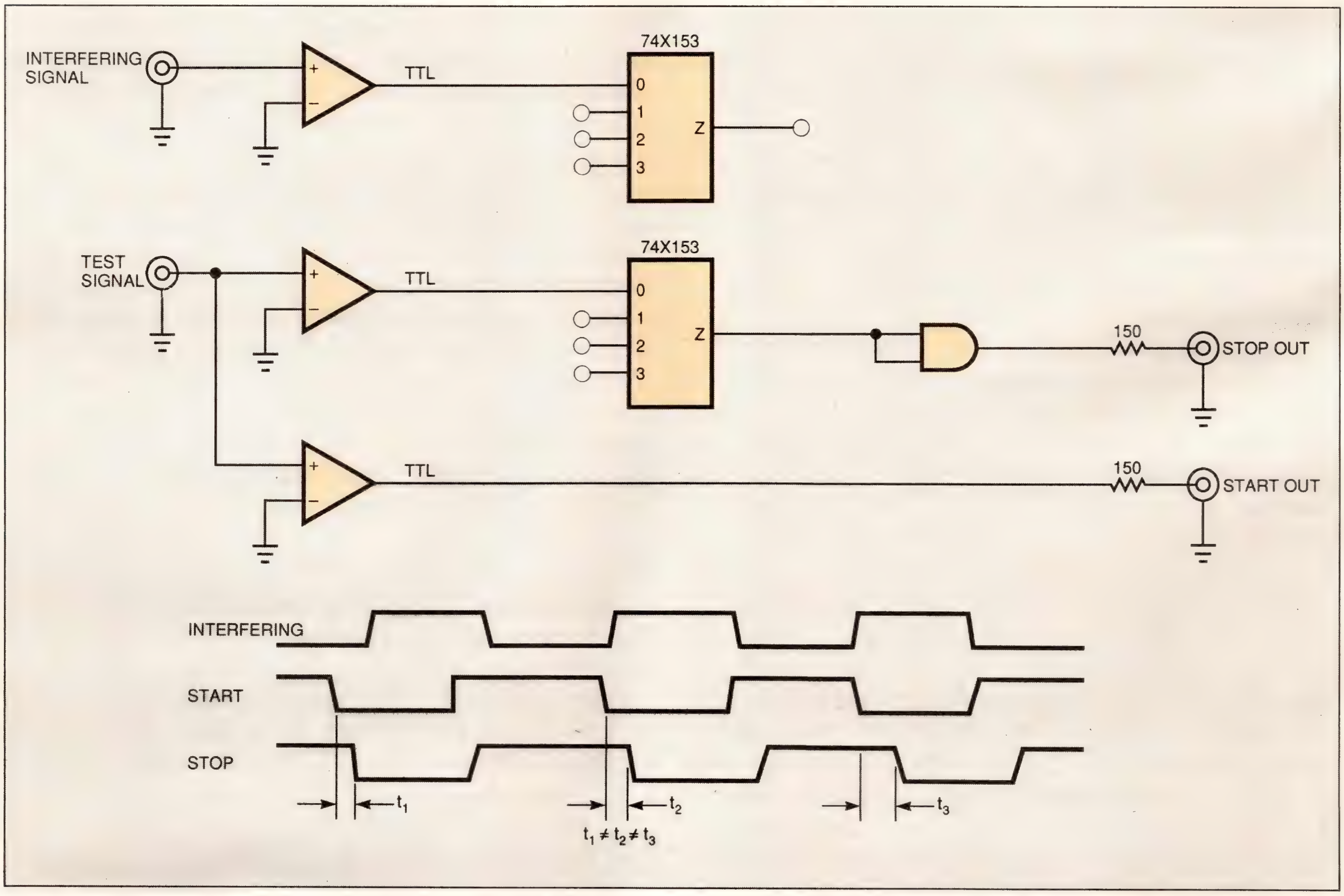


Fig 7—This setup was used *to examine how crosstalk between sections of high-speed CMOS chips affects the chips' propagation delay.*

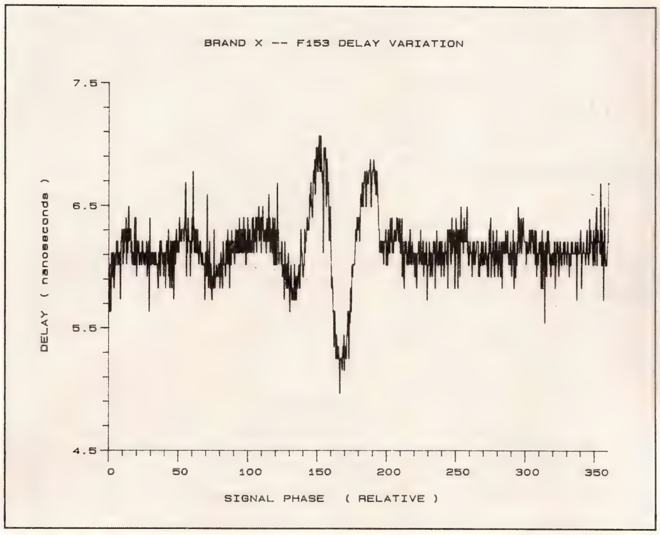


*Fig 8—**On one brand of 74F153,** the delay changed by approximately ±25% when an edge on an interfering signal (connected to a separate gate structure on the chip) neared coincidence with an edge on a signal connected to the structure under test.*

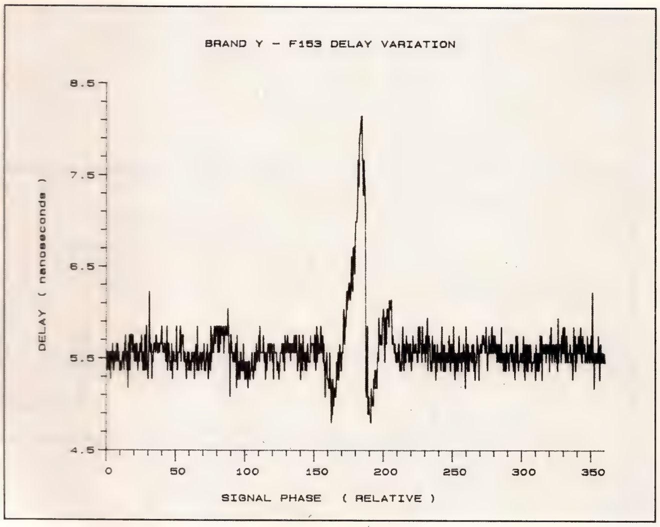


*Fig 9—**When subjected to the same conditions** as the part whose response is shown in **Fig** 8, another brand of 74F153 behaved quite differently.*

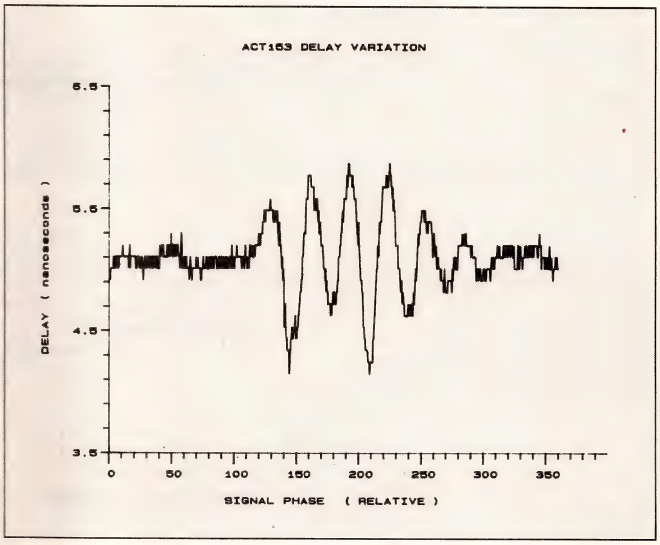
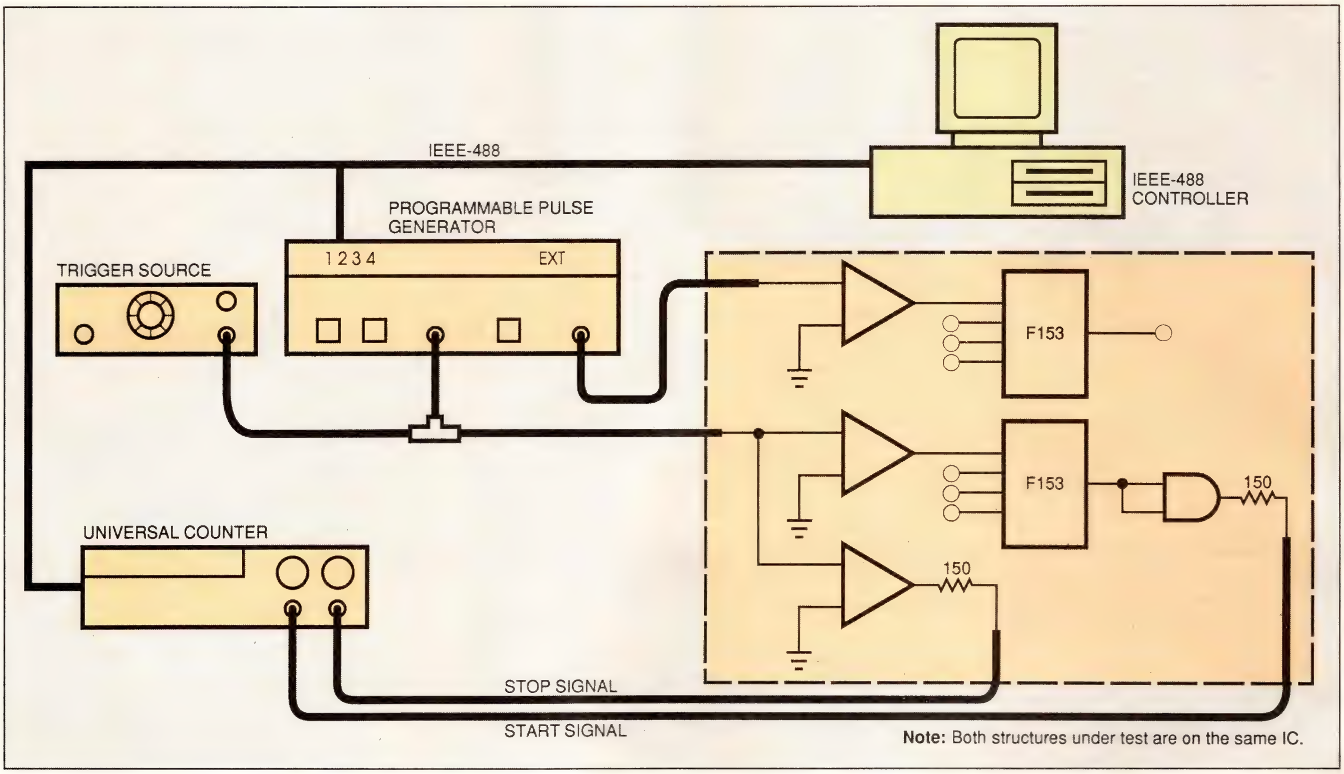


*Fig 10—**A 74ACT153 showed the effects of crosstalk** over a wider range of interfering-signal phase than did either tested brand of 74F153. (On the 74ACT153, you could see the effects of crosstalk when the interfering signal edge was further in time from the edge on the signal connected to the structure under test.)*

the circuits' gain, frequency slew rate, and post-tuning drift. Conventionally, engineers characterized these products using a time-consuming multicycle scheme based on a counter and an IEEE-488-programmable delay generator. Today, you can verify the performance of many of these parts in a single-shot test, using only a high-speed precision counter in the setup of **Fig 5. Fig 6** details the frequency-vs-time characteristic of a test VCO; the test also demonstrates how frequency-domain analysis can uncover problems difficult or impossible to find using alternative methods. During initial testing of the circuit, the designer noted a small perturbation at precisely 5 MHz on the rising edge of the frequency plot. He traced this deviation to injection locking of the VCO by a crystal-controlled oscillator on the same board. Detecting and solving this problem would have been extremely difficult without a counter. The capture and settling time of phase-locked loops are other important parameters that you can easily characterize with frequency-domain sampling.

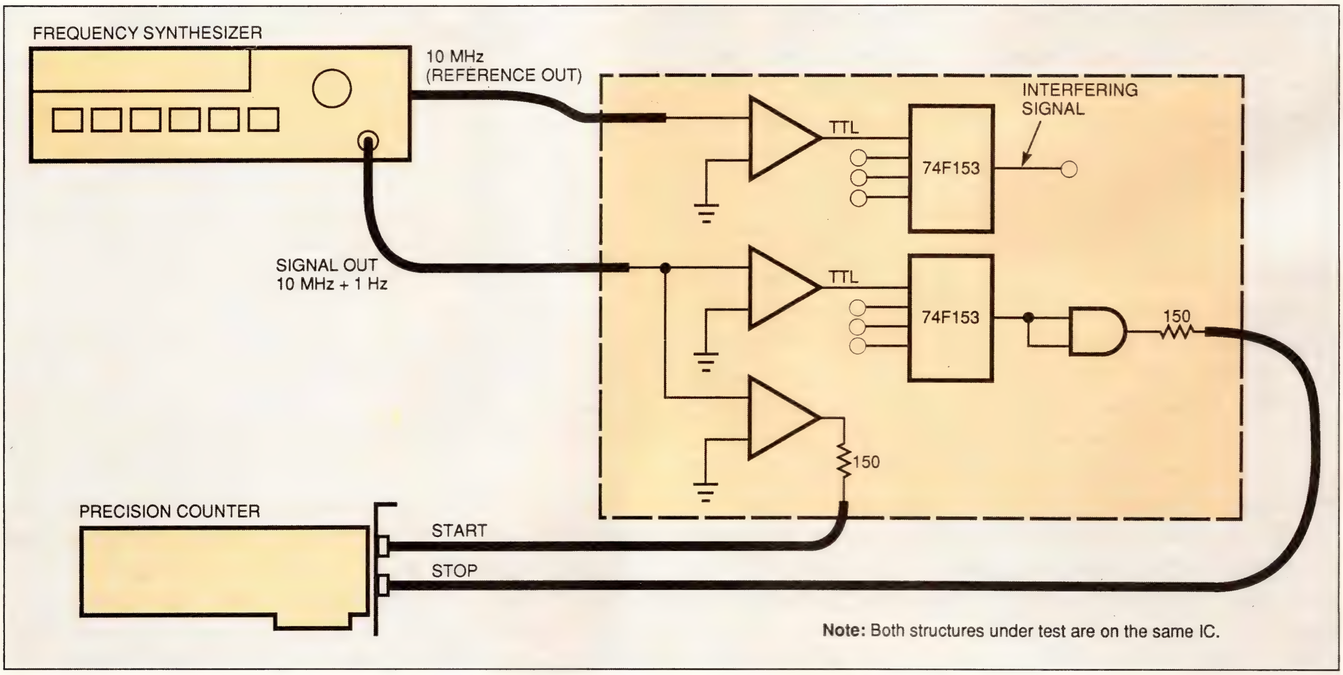
A digital-design engineer in need of a diagnostic tool will most often reach for a logic analyzer or a scope. In some cases, however, he should choose a precision universal counter instead, because the counter can yield data unobtainable with more traditional instruments.

The recent debate over high-speed CMOS pinouts may help you realize that logic gates are not as deterministic as you might have thought. Neither a first-order model of a logic gate nor a device data book would lead you to suspect that crosstalk between the various portions of an IC could cause significant variations in a fundamental property, such as propagation delay. Furthermore, crosstalk effects can vary between manufacturers of supposedly identical parts. In the bygone era of slow TTL and CMOS gates, a few nanoseconds of propagation-delay variation mattered



Note: Both structures under test are on the same IC.

Fig 11—You can build a crosstalk-measurement *setup from a trigger generator, a programmable pulse generator, a conventional universal counter, and an IEEE-488 controller.*



Note: Both structures under test are on the same IC.

Fig 12—An alternative crosstalk-measurement *setup uses a frequency synthesizer and a high-performance counter card that plugs into the IBM PC bus.*

Counter measures quickly with high resolution

The GT200 counter/timer, from Guide Technology, provides a number of features that make it especially suitable for the testing described in this article.

First, it provides high resolution in both frequency- and time-measurement modes. In time-interval measurement, the resolution is 100 psec for a single-shot measurement. When measuring frequency, its resolution is 10 digits with a 1-sec gate time. Translated into English, the last specification means that even at 1000 measurements/sec, the counter/timer can provide better than 1-ppm frequency resolution.

Second, the counter/timer can provide as many as 2300 readings/sec in time-measurement modes, and as many as 1400 readings/sec when measuring frequency.

Third, it simplifies high-speed data-acquisition tasks through built-in pacing. It can acquire more than 50,000 measurements at intervals programmable from less than 1 msec to more than 3200 sec.

Fourth, the GT200 comes with graphing capability, which allows it to quickly and painlessly display acquired data on a monitor.

Finally, and possibly most surprising, the counter/timer is an add-in card for IBM PC-compatible computers. It delivers the speed and precision of much more expensive stand-alone universal counters at a price of $1495.

A GT200 operating from its virtual front panel performed all of the tests described in the article. The counter/timer required no programming. Furthermore, all of the plots were generated by graphing routines integrated with the front-panel software.

little. Today, with 15-nsec CMOS static RAMs and several 5-nsec logic families, small delay variations can make or break a design. As you will see, gate-delay variations are not merely second-order effects that interest only academics; these delay variations can constitute a significant percentage of the data-sheet specification. **Figs 8**, **9**, and **10** show that the peak-to-peak variation can exceed 30% of the nominal gate delay.

In the first analysis, we tested several high-speed, TTL-compatible, dual 4-input multiplexers to ascertain the level of delay variation caused by crosstalk within the parts. We characterized both 74ACT153 and 74F153 parts. We measured the delay through one half of the part while we sent an asynchronous interference signal through the second half (**Fig 7**). **Figs 8**, **9**, and **10** show the delay "signatures" for three types of parts. These plots show delays vs the relative phase of the second, interfering, signal. (If there were no crosstalk, the plots would show only minor deviations from a straight line.) Note that when both outputs are changing states, there is a dramatic effect on delay. The strongest coupling seems to occur between the rising edges of the interfering signal and the falling edges of the test signal.

The most obvious technique for gathering the delay data is to construct the small system shown in **Fig 11**. The IEEE-488 controller varies the pulse-generator delay so that the interfering signal transition sweeps across the main signal. The controller also gathers the time data from the counter and plots the result. This technique does not place stringent requirements on the counter, because the instrument can use time-interval averaging. However, the technique does demand both an IEEE-488-programmable precision delay generator and a significant programming effort.

An alternative setup can significantly speed crosstalk measurements and eliminate the need for costly pulse generators and lengthy program development. However, this technique, which resembles equivalent-time sampling in DSOs, makes new demands on the universal counter. As in many of the previous examples, the counter must now deliver both exceptional single-shot time-interval accuracy and high-speed data acquisition. **Fig 12** shows the setup, which uses two signal sources with a small difference in frequency. One signal drives the measured path and the second drives the interference path. The slight frequency offset causes the interfering signal to sweep across the main signal in a known manner; the sweep period is equal to the reciprocal of the frequency offset. For example, if the main signal were 10 MHz and the interfering signal were 10.000002 MHz, the sweep would take 0.5 sec. Although the relative phase of the two signals is continuously changing, the rate is slow enough that the counter can acquire a large number of data points in a single sweep. We acquired the data shown in the sample plots by taking 1000 samples using a base frequency of 10 MHz and an offset of 1 Hz. The time spacing between samples was 100 psec:

$$\text{delta\_t} = \frac{(\text{base\_signal\_periodoffset\_freq})}{\text{sample\_rate}}.$$

In theory, you can achieve arbitrarily fine time resolution if the frequency offsets are very small. However, the short-term stability of the sources will ultimately limit the resolution.

During the past decade, active delay lines have increased in popularity as circuit timing requirements have become more precise. Although the delay lines provide good performance in most applications, designers must know the devices' limitations so they can characterize parts used in especially critical circuits. In this final set of experiments, we tested a delay line

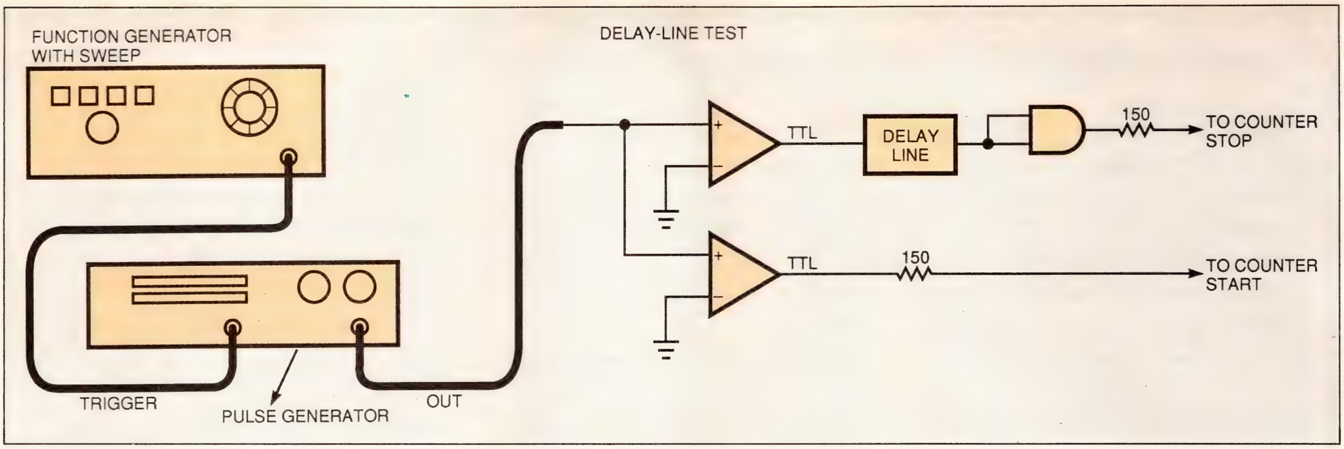


***Fig 13—To characterize delay lines** with a counter, you need to add only a sweep/function generator.*

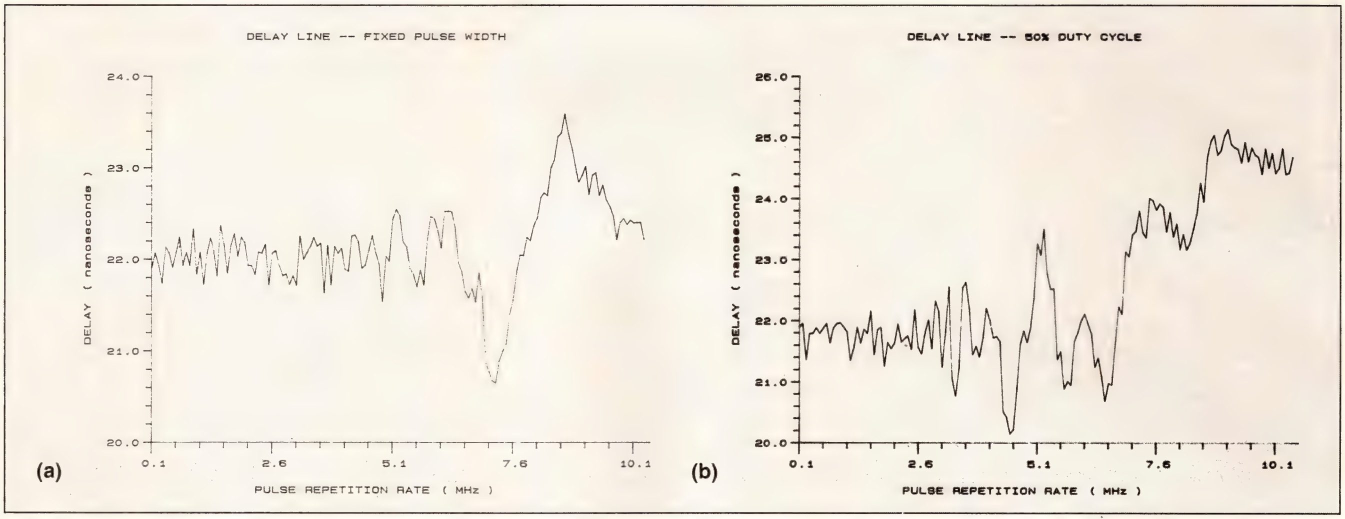
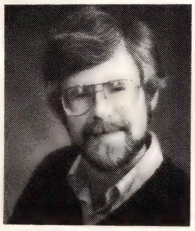


***Fig 14—When its input signal is a pulse** of constant width, an active delay line produces a delay, **(a)**, that is moderately sensitive to the pulse frequency, but when the signal is a square wave, **(b)**, the delay's sensitivity to the input-signal frequency is much greater.*

for its sensitivity to changes in both signal frequency and pulse width. The setup, shown in **Fig 13**, used a function generator with sweep capability to generate the basic test signal. In the first variation, we connected the pulse generator in the signal path to provide the desired constant pulse width. We used the counter to acquire delay measurements as the function generator swept from 0.1 MHz to 10 MHz. **Fig 14a** shows that the delay line we tested is sensitive to repetition rates in excess of 6 MHz. In the second variation, we removed the pulse generator from the circuit and directly applied the function generator's square-wave signal to the delay line, so that the pulse width changed as the frequency changed. **Fig 14b** shows that the delay line was more sensitive to simultaneous changes in pulse width and repetition rate than it was to changes in rate alone.

Although many engineers view frequency counters as archaic and, therefore, uninteresting, recent advances in the technology make possible applications that classical counters couldn't handle. Far from being "straw men" designed to showcase the capabilities of instruments that combine high resolution with fast measuring speed, these applications are significant to engineers throughout the electronics field. Furthermore, the examples presented only scratch the surface of what you can accomplish with these new—and affordable—instruments. **EDN**

Author's biography



Lewis W Masters is vice president of engineering, responsible for hardware development of PC-compatible instrumentation, at Guide Technology Inc, where he has worked for approximately two years. He previously developed counter/timer products for Hewlett-Packard. He holds a BSME from the University of Maryland and an MSEE from the University of California at Santa Barbara. In his spare time, he enjoys woodworking, making furniture, and automotive-repair work.

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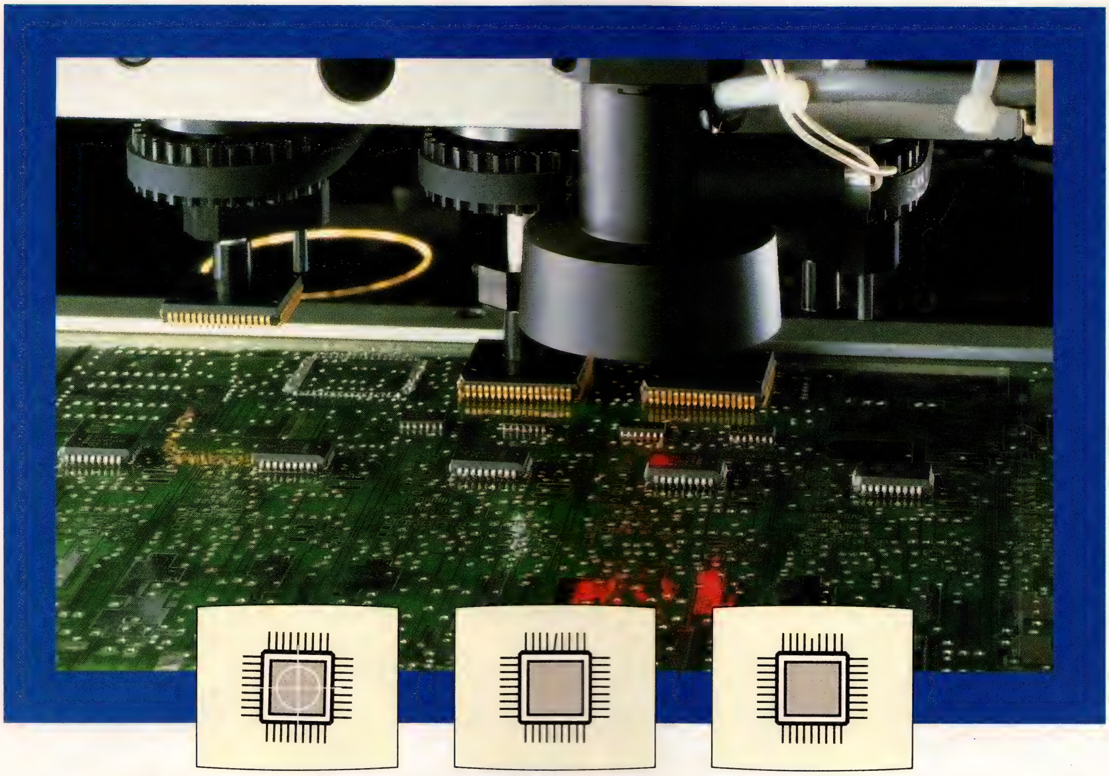

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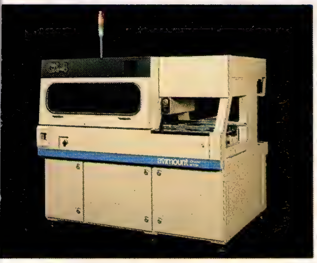

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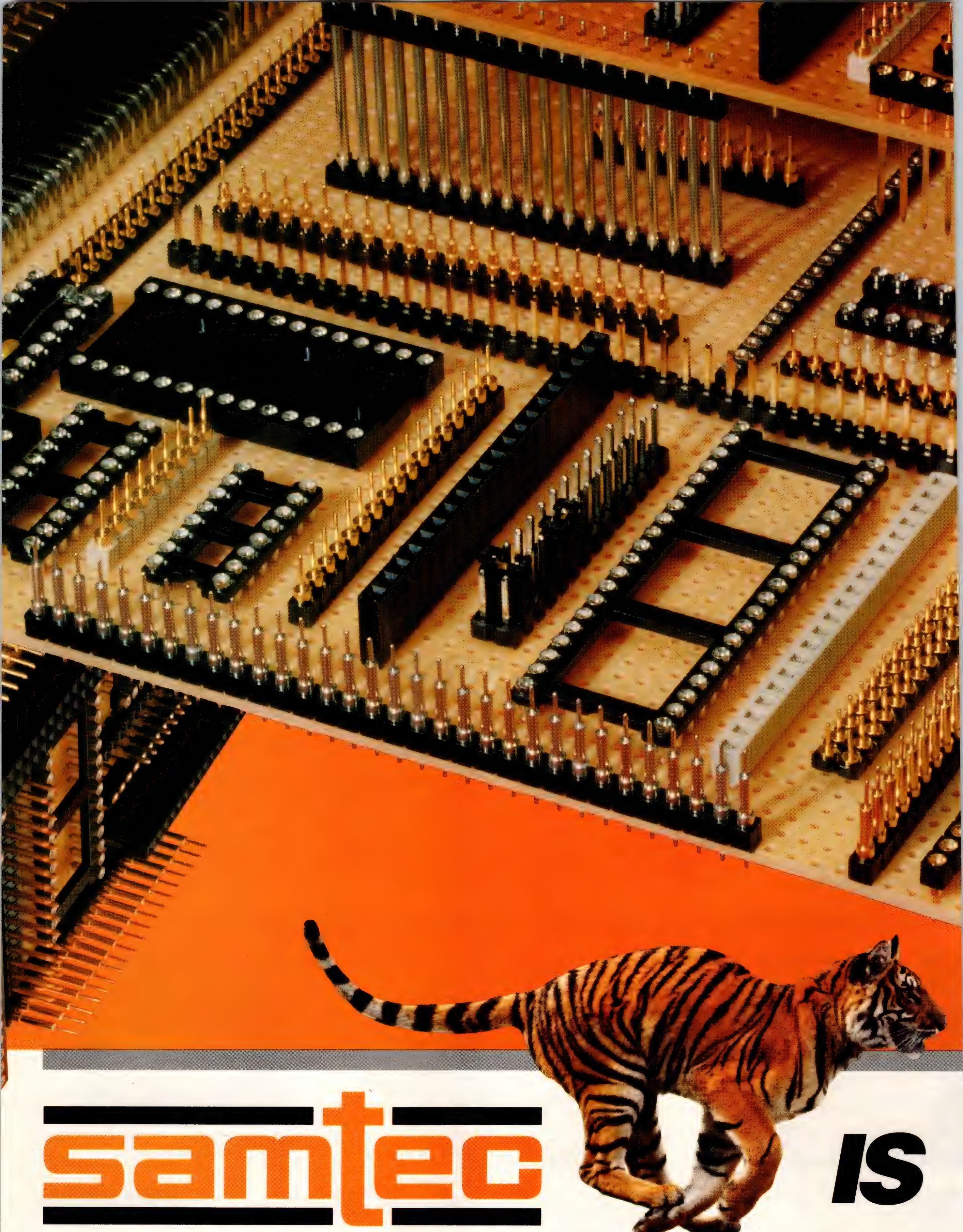

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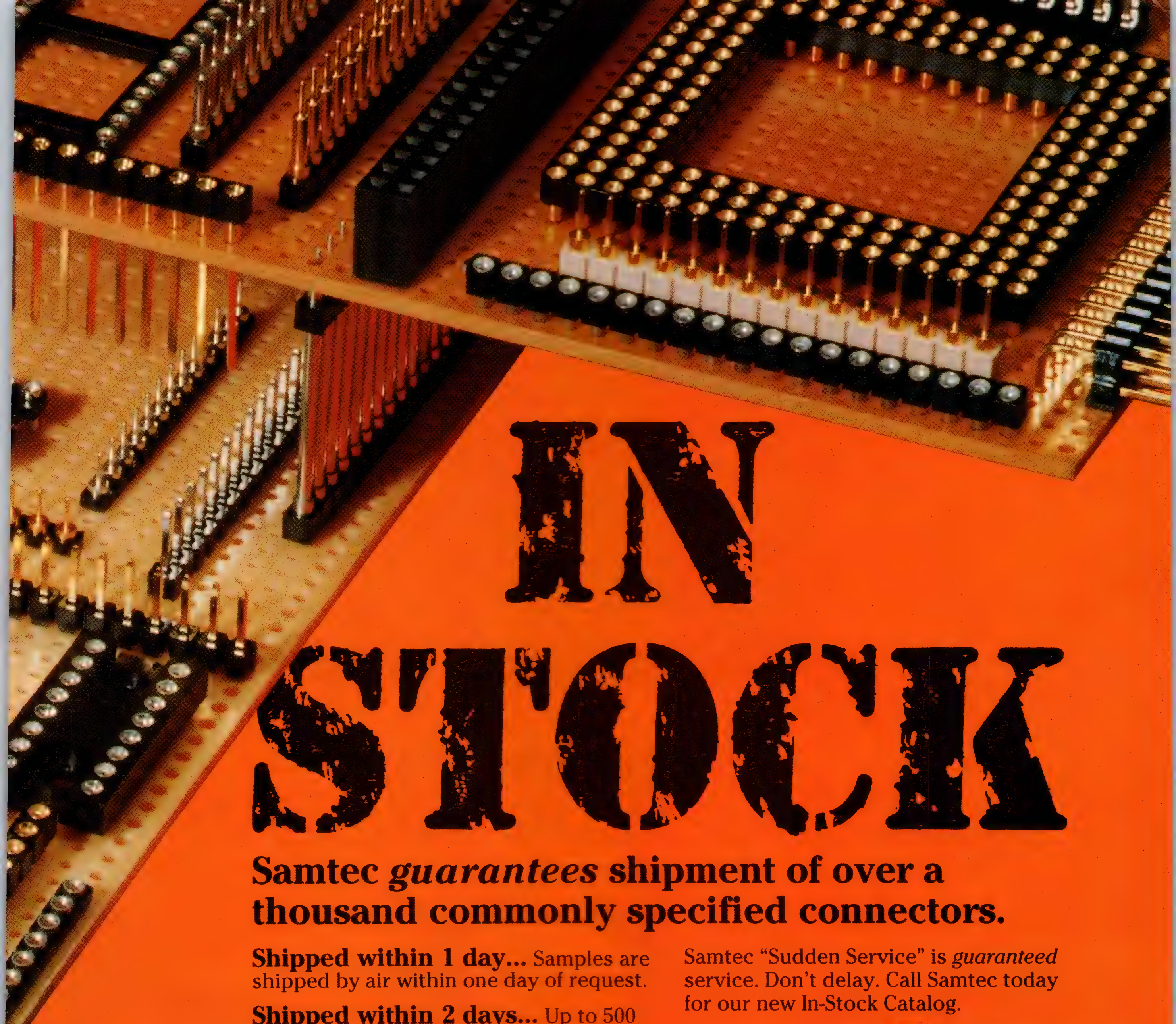

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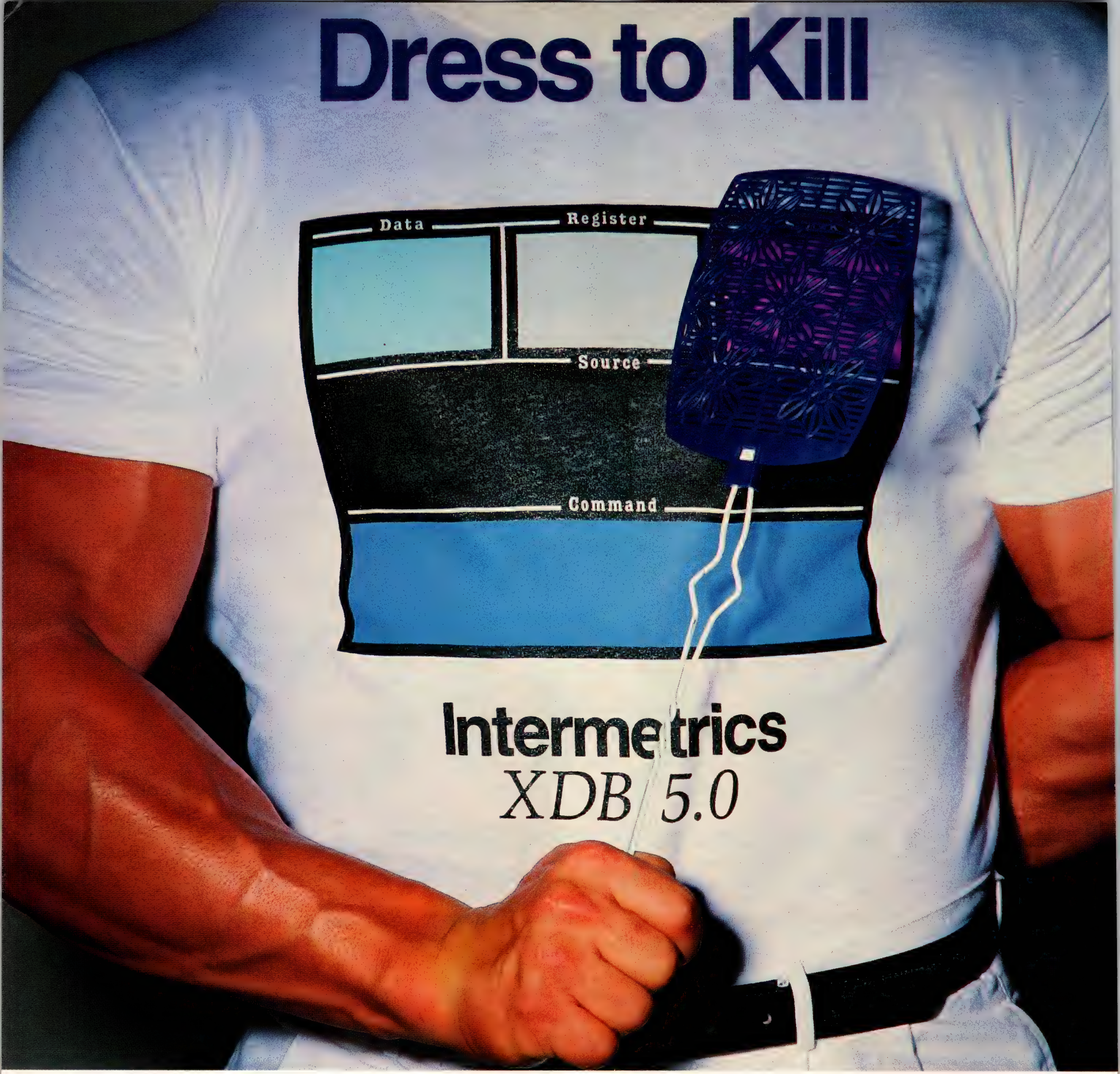

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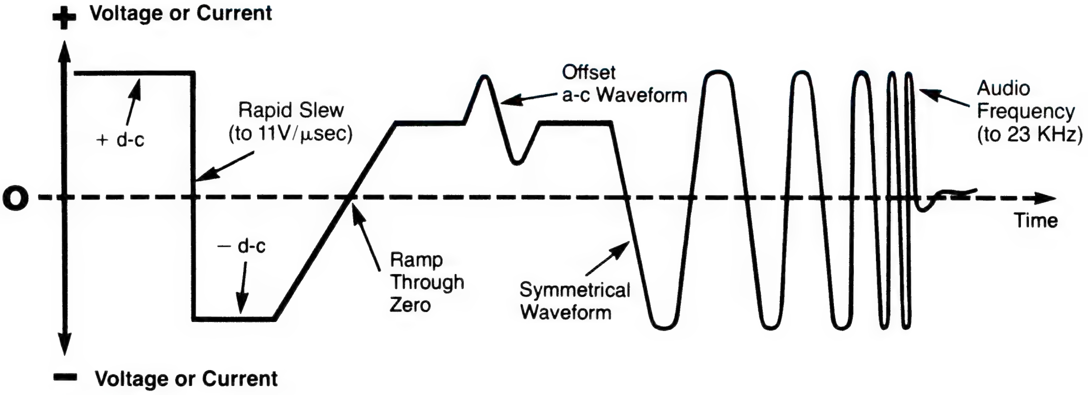

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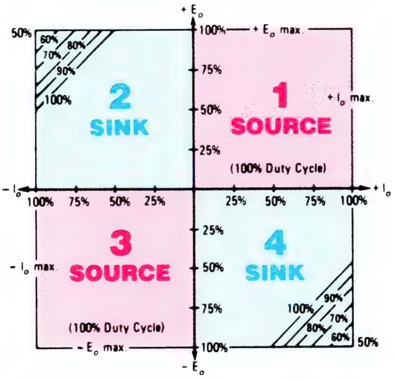
BOP are bidirectional. Their *single* output can be both positive or negative with no transition as they pass through zero. BOP, therefore, can reproduce both the *sense,* as well as the *magnitude,* of their input. BOP are 4-quadrant devices able to *sink* approximately 50% of the power that is sourced. (See plot.)



Output Source-Sink plot
The values for ± $E_{o\,max}$ and $I_{o\,max}$ are listed in the model table.

This means, among other things, that BOP can be used to emulate the charge-discharge cycle of batteries — or to drive batteries, or to drive energy storage elements like inductors. (To drive large inductors, however, BOP must be slowed down so that they remain stable. Terminals are provided in the user port for an external capacitor to control bandwidth.)

BOP are test system drivers. Plug in the optional IEEE-488 card (called "BIT"), and you're on the bus listening for ASCII strings to set voltage and current and polarity.

Connect the BOP, instead, to Kepco's MATE-verified TMA, called TLD 488-16, and the BOP can be one of up to 16 power instruments communicating in the Control Intermediate Interface Language (CIIL). As a device driver in your test stand, you can rapidly sequence or step the BOP through a complex series of d-c levels and/or a-c waveforms.

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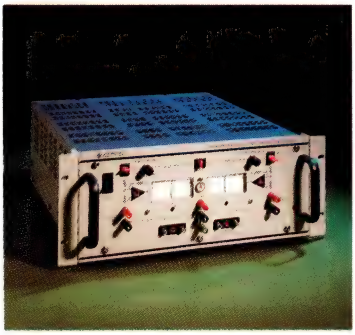

Model BOP 1000M

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DYNAMIC SPECIFICATIONS

MODEL	BANDWIDTH (d-c to f_{-3dB}) KHz (minimum) Mode V	I	RISE & FALL TIME 10%-90% µsec (maximum) Mode V	I	LARGE SIGNAL FREQUENCY (min) RESPONSE, KHz Mode V	I	SLEWING RATE (minimum) Mode V	I	RECOVERY STEP LOAD µsec (maximum) Mode V	I
100 WATT										
BOP 50-2M	18	12	20	30	17	13	5V/µsec	0.15A/µsec	25	10
BOP 100-1M	18	11	17	22	18	11	11V/µsec	70mA/µsec	40	25
200 WATT										
BOP 20-10M	18	6	20	60	17	7	2V/µsec	0.4A/µsec	80	20
BOP 36-6M	16	13	20	27	15	14	3V/µsec	0.5A/µsec	50	35
BOP 50-4M	23	14	14	25	15	11	4.5V/µsec	0.25A/µsec	40	30
BOP 72-3M	20	15	18	26	17	12	10V/µsec	0.15A/µsec	30	30
BOP 100-2M	22	15	18	26	17	12	10V/µsec	0.15A/µsec	30	30
BOP 200-1M	3.8	1.8	70	150	3.5	1.8	4V/µsec	10mA/µsec	150	120
400 WATT										
BOP 20-20M	9.5	10	35	35	8	10	1V/µsec	1.25A/µsec	100	75
BOP 36-12M	20	10	16	30	19	10	4V/µsec	0.75A/µsec	50	30
BOP 50-8M	24	10	14	35	24	11	7.5V/µsec	0.5A/µsec	40	30
BOP 72-6M	19	9.5	18	40	20	11	9V/µsec	0.4A/µsec	50	20
BOP 100-4M	18	14	22	30	16	10	10V/µsec	0.25A/µsec	40	30
HIGH VOLTAGE										
BOP 500M	2	1.3	165	275	2	2	6V/µsec	1mA/µsec	100	125
BOP 1000M	1	0.64	330	550	0.5	0.5	3V/µsec	0.13mA/µsec	100	250

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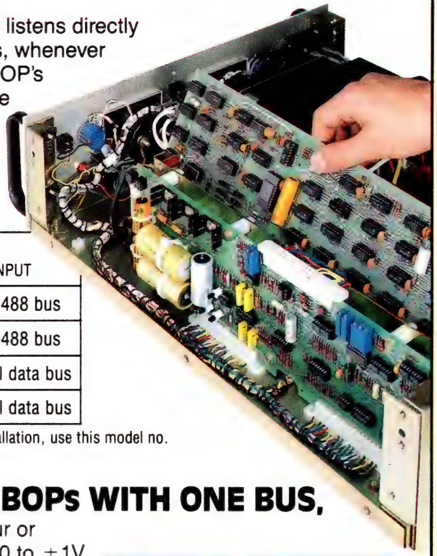

With a BIT Digital Interface card installed, your low voltage BOP listens directly to digital instructions from the IEEE 488 bus, or a parallel data bus, whenever it hears "remote enable." These cards will control either the host BOP's voltage channel (while limiting current), or its current channel (while limiting voltage). Available in two styles: for the IEEE bus, or for parallel data buses, and with a hexadecimal or a BCD format. BOP 500M and BOP 1000M do not have provision for the BIT card.

SUFFIX(1)	MODEL(2)	DATA FORMAT	RESOLUTION Principal Channel	Limit Channel	INPUT
—488-B	BIT 488-B	ASCII/Hex	12 Bits (binary)	8 Bits (binary)	IEEE-488 bus
—488-D	BIT 488-D	ASCII/Decimal	3-Digit (BCD)	2-Digit (BCD)	IEEE-488 bus
—500-B	BIT 500-B	Hexadecimal	12 Bits (binary)	8 Bits (binary)	parallel data bus
—500-D	BIT 500-D	Decimal	3-Digit (BCD)	2-Digit (BCD)	parallel data bus

(1)To order factory-installed interface, add to BOP model no. (2)To order separately for field installation, use this model no.

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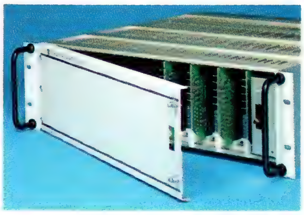

SNR Housings

MODEL	HOLDS
SNR 488-4	4 Cards
SNR 488-8	8 Cards

Interface cards

MODEL	DATA FORMAT	RESOLUTION
SN 488-B	Hex	12-bit binary
SN 488-D	Decimal	3-digit BCD

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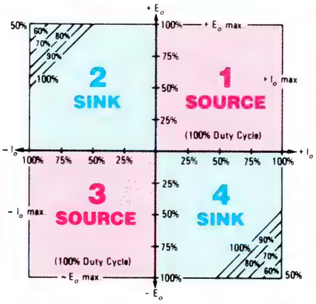
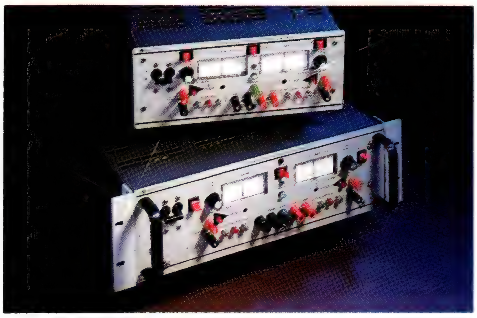
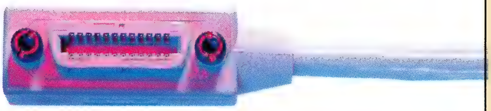


Output source-sink plot



...produce a stabilized
voltage or a
stabilized current,
either positive or
negative, a-c or d-c,

...and get on the bus
without fuss.



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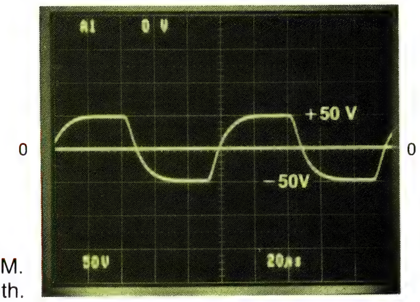

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MODEL TABLE

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			VOLTAGE CHANNEL G_V (V/V)	CURRENT CHANNEL G_I (A/V)	VOLTAGE MODE		CURRENT MODE		
	E_o max.	I_o max.			SERIES R	SERIES L	SHUNT R	SHUNT C	
100 WATT ($^3/_4$ rack)	**Size:** $5\frac{7}{32}$″ H x $12\frac{17}{32}$″ W x $17\frac{9}{64}$″ D(3) (132.6mm H x 318.3mm W x 435.4mm D) **Shipping Weight:** 48 lbs. (21.8 kg.)								
BOP 50-2M	± 50V	± 2A	5.0	0.2	0.5 mΩ	100μH	50 kΩ	0.05μF	2.9
BOP 100-1M	± 100V	± 1A	10.0	0.1	2.0 mΩ	200μH	100 kΩ	0.05μF	2.9
200 WATT ($^3/_4$ rack)	**Size:** $5\frac{7}{32}$″ H x $12\frac{17}{32}$″ W x $17\frac{9}{64}$″ D(3) (132.6mm H x 318.3mm W x 435.4mm D) **Shipping Weight:** 51 lbs. (23.1 kg.)								
BOP 20-10M	± 20V	± 10A	2.0	1.0	40 μΩ	50μH	20 kΩ	0.1μF	5.5
BOP 36-6M	± 36V	± 6A	3.6	0.6	120 μΩ	50μH	36 kΩ	0.1μF	5.1
BOP 50-4M	± 50V	± 4A	5.0	0.4	0.25 mΩ	100μH	50 kΩ	0.05μF	4.8
BOP 72-3M	± 72V	± 3A	7.2	0.3	0.48 mΩ	200μH	72 kΩ	0.05μF	5.1
BOP 100-2M	± 100V	± 2A	10.0	0.2	1.0 mΩ	200μH	100 kΩ	0.05μF	4.8
400 WATT (Full rack $5^1/_4$″)	**Size:** $5\frac{7}{32}$″ H x $16\frac{15}{32}$″ W x $20\frac{5}{64}$″ D(3) (132.6mm H x 418.3mm W x 510mm D) **Shipping Weight:** 90 lbs. (40.8 kg.); BOP 200-1M: 85 lbs. (38.6 kg.)								
BOP 20-20M	± 20V	± 20A	2.0	2.0	20 μΩ	50μH	20 kΩ	0.2μF	11.2
BOP 36-12M	± 36V	± 12A	3.6	1.2	60 μΩ	50μH	36 kΩ	0.2μF	10.7
BOP 50-8M	± 50V	± 8A	5.0	0.8	125 μΩ	100μH	50 kΩ	0.15μF	9.6
BOP 72-6M	± 72V	± 6A	7.2	0.6	240 μΩ	200μH	72 kΩ	0.1μF	10.9
BOP 100-4M	± 100V	± 4A	10.0	0.4	500 μΩ	200μH	100 kΩ	0.1μF	9.2
BOP 200-1M(2)	± 200V	± 1A	20.0	0.1	4.0 mΩ	600μH	200 kΩ	0.03μF	4.8
HIGH VOLTAGE (Full rack 7″)	**Size:** $6\frac{31}{32}$″ H x $16\frac{1}{2}$″ W x $17\frac{5}{64}$″ D(3) (177.0mm H x 419.1mm W x 433.8mm D) **Shipping Weight:** 65 lbs. (29.5 kg.)								
BOP 500M	± 500V	± 80mA	50	0.008	0.05 Ω	10 mH	100 MΩ	0.02 μF	3.8
BOP 1000M	± 1000V	± 40mA	100	0.004	0.2 Ω	10 mH	400 MΩ	0.01 μF	3.8

(1)For factory installed digital interface add appropriate suffix. Not available to High Voltage models

(2)BOP 200-1M is rated for 200 Watts. (3)Add $2\frac{1}{2}$″ (63.5mm) for connector protrusion

STATIC SPECIFICATIONS

LOW VOLTAGE MODELS

INFLUENCE QUANTITY		OUTPUT EFFECTS(1)				PREAMPLIFIER OFFSETS		REFERENCE ± 10V
		VOLTAGE MODE		CURRENT MODE				
		TYP	MAX	TYP	MAX	ΔE_{io}	ΔI_{io}	
SOURCE (min.-max.)		<0.0005%	0.001%	<0.002%	0.005%	<5μV	<1nA	<0.0005%
LOAD (No load-full load)		<0.001%	0.002%	<0.5mA	1mA	—	—	<0.0005%
TIME (8-hour drift):		<0.005%	0.01%	<0.01%	0.02%	<20μV	<1nA	<0.005%
TEMP., (Per °C)		<0.005%	0.01%	<0.01%	0.02%	<20μV	<1nA	<0.005%
RIPPLE and NOISE:(2)	rms	<1mV	3mV	<0.01%	0.03%	—	—	—
	p-p(3)	<10mV	30mV	<0.1%	0.3%	—	—	—

HIGH VOLTAGE MODELS

INFLUENCE QUANTITY		OUTPUT EFFECTS(4)		PREAMPLIFIER OFFSETS		REFERENCES
		VOLTAGE MODE	CURRENT MODE	ΔE_{io}	ΔI_{io}	
SOURCE VOLTAGE (min.-max.)		<0.0005%	<0.0005%(5)	<5μV	<1nA	<0.0005%
LOAD (No load-full load)		<0.0005%	<0.005%	—	—	<0.0005%
TIME (8-hour drift)		<0.01%	<0.01%	<20μV	<1nA	<0.005%
TEMPERATURE (Per °C)		<0.01%	<0.01%	<20μV	<1nA	<0.005%
RIPPLE and NOISE(2)	rms	<10mV	<25μA(6)	—	—	<10μV
	p-p BOP 500M	<100mV(3)	<25μA(6)	—	—	<100μV
	p-p BOP 1000M	<200mV(3)	<200μA(6)	—	—	<100μV

(1)Output effects, expressed as a percentage, are referred to the maximum rated output voltage and current.

(2)Measured with the common terminal grounded so that the common mode current does not flow through the load.

(3)Peak-to-peak ripple is measured over a 20Hz to 10MHz bandwidth.

(4)Specifications are expressed as a *percent-of-setting* for the output range 10% to 100%. Below 10% output, specification limit is the rated percentage of the 10% output setting.

(5)Or 0.2μA, whichever is greater.

(6)For frequency components in the bandwidth of the current stabilizer. Beyond cutoff, noise will appear as a voltage component equal to the rated voltage mode noise.

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SPECIFICATIONS

INPUT

Input voltage:
low voltage models — selectable, 95-113, 105-125, 190-226, or 210-250V a-c, 50-65 Hz, single phase.

high voltage models — selectable, 105-125V a-c, 210-250V a-c, 50-65Hz.

Input current:
see model table.

Time delay:
high voltage models — 30 seconds.

OUTPUT

Output voltage and current:
low and high voltage models — continuously adjustable or programmable, from 100% of the negative spec to 100% of the positive spec.

Control voltage/current:
low and high voltage models — local: 10-turn zero-center potentiometer on front panel. remote: −10 to +10V signal.

Remote error sensing:
low and high voltage models — 0.5V per load wire.

GENERAL

Front panel LEDs:
low and high voltage models — Voltage, Current, Voltage$_{\text{limit}}$, Current$_{\text{limit}}$.
Remote On (low voltage models).
Ready (high voltage models).

Cooling:
low voltage models — built-in fan exhausts air to rear.

high voltage models — natural convection.

d-c output terminal:
low and high voltage models — front signal/output: binding posts. rear output: barrier strip.

Rear user port:
low voltage models — 50 terminal connector.

high voltage models — 30 terminal connector.

Meters:
low and high voltage models — voltmeter and ammeter, 2$\frac{1}{2}$″ ±2%, zero-centered.

Mode flag:
low and high voltage models — TTL logic signals corresponding to front panel LEDs available at user port.

Isolation:
low and high voltage models — output may be floated up to 500V off ground; common mode current: 5μA rms, 50μA p-p at 115V a-c.

Series operation:
low and high voltage models — to the 500V limit of the isolation voltage; master/slave operation is possible.

Parallel operation:
low and high voltage models — current sharing; use master/slave connection.

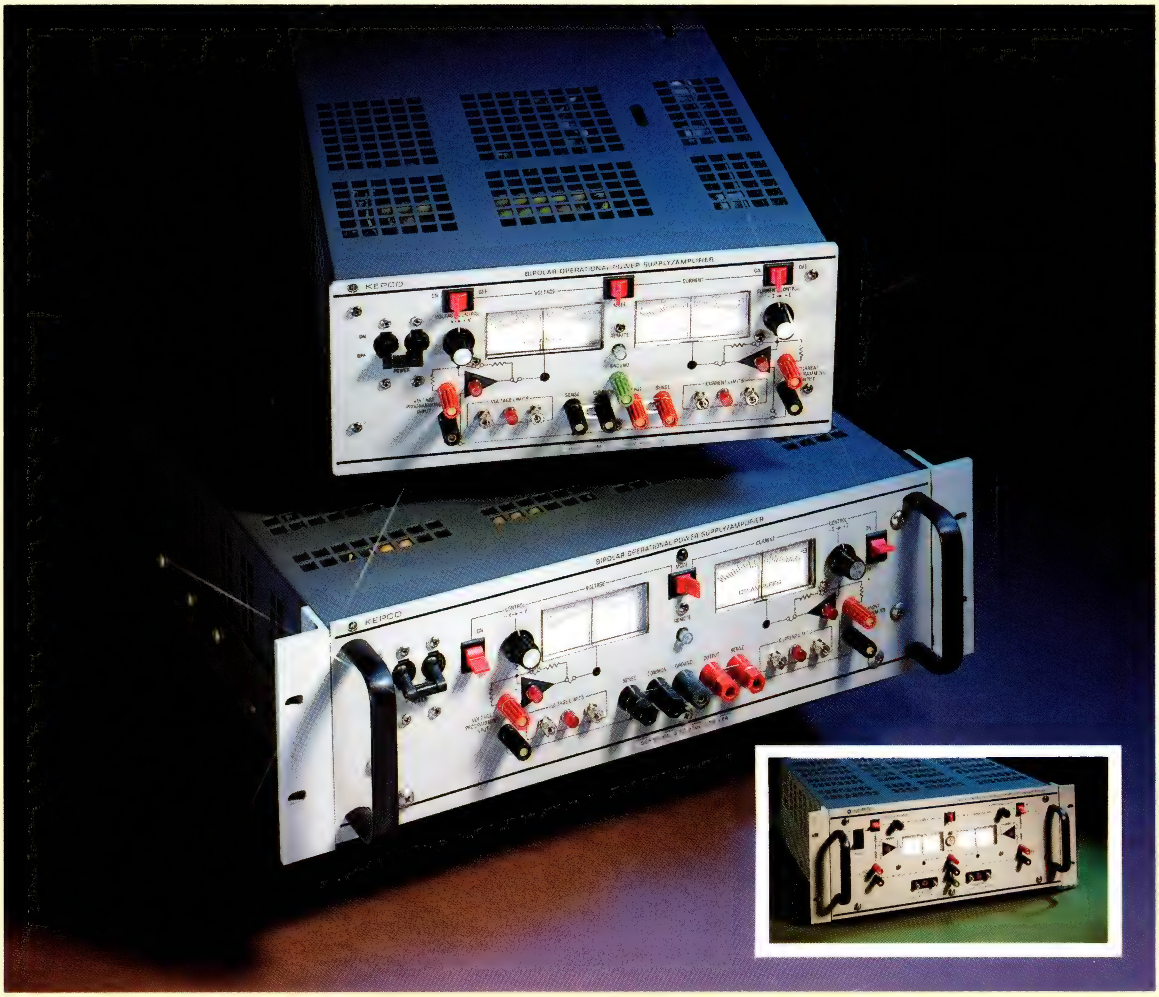
Temperature:
low voltage models —
storage: −40°C to +85°C.
operating: 0°C to +55°C.
high voltage models —
storage: −40°C to +85°C.
operating: −20°C to +65°C.

Mounting:
100W and 200W models are $\frac{3}{4}$ rack size, each mount with Kepco model RA 37 using RFP 37-1 filler panel.

400W models are full rack 5$\frac{1}{4}$″ x 19″ to mount directly (ears provided). Note: The BOP 200-1M is a full rack 5$\frac{1}{4}$″ x 19″ panel.

High voltage models are full rack 7″ x 19″ panels to mount directly in a 19″ rack (ears provided).

Low voltage BOP Power Managers, $\frac{3}{4}$ rack and full rack sizes. Inset shows Model BOP 1000M.


KEPCO
BIPOLAR OPERATIONAL POWER SUPPLY/AMPLIFIER
KEPCO
BIPOLAR OPERATIONAL POWER SUPPLY/AMPLIFIER

Kepco's Series BOP power supplies are "MATE-verified" for use in Modular Automatic Test Equipment that is addressed in the (CIIL) Control Interface Intermediate Language.

Kepco's TLD 488-16 interactive digital interface is an IEEE-488-driven talker-listener that has been verified as a TMA (Test Module Adapter) for Kepco's ATE(1) and BOP power supplies.

On October 1, 1987 Kepco's TLD officially achieved "MATE-verified" status. The certificate shown was issued by the MATE program office, Kelly AFB, Texas.

Kepco BOP Power Manager controlled by computer via Kepco TLD 488-16 Interactive Digital Interface.

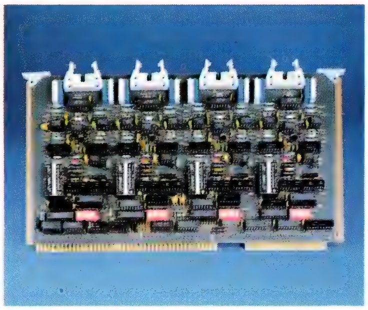
The TLD 488-16 responds to commands in CIIL (Control Interface Intermediate Language) over the IEEE-488 bus from your computer or digital controller, and passes them along to the BOPs under its control. It can control up to 16 BOPs at once, and if one of them cannot obey a command, it sends back a flag which the TLD 488-16 translates into CIIL and passes along to the controller as an "error message".

The error messages it can send are:

Crowbarred
Overload
Voltage comparison error
Current comparison error
Voltage out of range
Current out of range
Relay not open*
Relay not closed
Device not present
Invalid command
No devices selected
Received incomplete message

You can give your commands to the TLD 488-16 directly in Volts and Amps, because it knows the voltage and current ranges of all the BOP Power Managers under its control, and can calculate what percentage of full scale a given voltage or current setting is.

The TLD 488-16 also controls Kepco Series ATE unipolar Power Managers.



PLUG-IN PROGRAM CARDS
(Standard Multibus Size)

The TLD 488-16 has provision for up to four (4) plug-in cards called TL 488-4A for Kepco's ATE power supplies or TL 488-4B for Kepco's BOP series bipolar power supplies. Each plug-in card can control the voltage and current function of up to four (4) power supplies. With a full complement of four (4) TL 488-4A or TL 488-4B, the system will control 16 individual, isolated, power supplies.

---

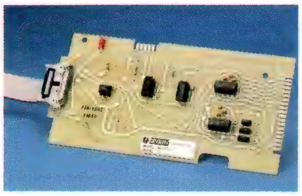
* *Refers to Isolation Relays TLR 25 and TLR 200, which can be interposed between the power supply and the load, in accordance with MATE system requirements.*

(1) ATE are Kepco Unipolar Power Supplies. Please see brochure 146-1635.

For full information on the TLD 488-16 Digital Interface, write for KEPCO Brochure 146-1448.

INTERNAL INTERFACE TO CONNECT TLD 488-16 WITH ITS BOP POWER MANAGERS

The interface is called PCA X-3. This card plugs into the BOP (low voltage models) occupying the digital slot. The PCA X-3 has the connector to mate with the cable to the digital programmer TLD 488-16 and is used to identify the power supply and measure the output voltage and current. The measured values are compared with the programmed values to determine whether or not an error message is required. PCA X-3 and the TLD 488-16 are not used with the BOP 500M and BOP 1000M.



PCA X-3 with Interconnect Cable to the TLD 488-16

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Nonlinear components lower settling time of noise-reduction filters

Noise filtering often causes an increase in settling time, but the proper application of a nonlinear filter can speed data acquisition by 4 to 1 over simple RC filters.

Rod Burt and R Mark Stitt, *Burr-Brown Corp*

The most common method of improving S/N ratio is noise reduction by filtering. The attendant increase in settling time, however, can be a serious disadvantage in certain applications, such as high-speed data acquisition. A nonlinear filter is a simple way to achieve a 4-to-1 improvement in settling time over conventional filters.

First, consider the dynamics of a single-pole RC filter **(Fig 1a)**. Filtering reduces broadband or white noise by the square root of the bandwidth reduction, according to the following equations, where e_n is the total noise in V_{rms}, e_B is the broadband noise in $V/\sqrt{Hz}$, and f_1 to f_2 is the filter's frequency range in hertz:

$$e_n^2=\int_{f1}^{f2} e_B^2\,df=e_B^2\cdot f\Big|_{f1}^{f2},$$

and thus,

$$e_n=e_B\sqrt{f_2-f_1}.$$

These equations show that if you reduce the frequency range, f_2-f_1, by a factor of 100, the total noise decreases by a factor of 10.

Unfortunately, the settling time increases as the bandwidth decreases. For a single-pole filter, you can calculate the time needed for the signal to settle to any given accuracy using the following equations, where t_S is the settling time in seconds, % is the percent of accuracy at time t_S, and R_1C_1 is the RC time constant in ΩF. At time t_S,

$$\frac{V_{OUT}}{V_{IN}}=1-e^{-(t_S/R_1C_1)},$$

and

$$-\left(\frac{V_{OUT}}{V_{IN}}-1\right)100=\%.$$

Therefore,

$$t_s=-\ln\,(\%/100)\ R_1C_1.$$

To determine the number of time constants required for the signal to settle within 0.01%, simply calculate ln(0.01/100), which equals −9.2. Thus, it takes 9.2 RC time constants for an input step to settle to within 0.01% of its final value.

A simple, diode-clamped nonlinear filter **(Fig 1b)** can improve the settling time of a simple RC filter. When you initially apply a large input step to V_{in}, the filter capacitor, C_1, charges faster through the forward-biased diode's low impedance than it can through R_1. When the difference between the input and output voltages becomes less than the forward-biased diode's drop (about 0.6V), the diode stops conducting, and C_1

Most filters cause an increase in settling time, but longer settling times are a severe disadvantage for data-acquisition systems.

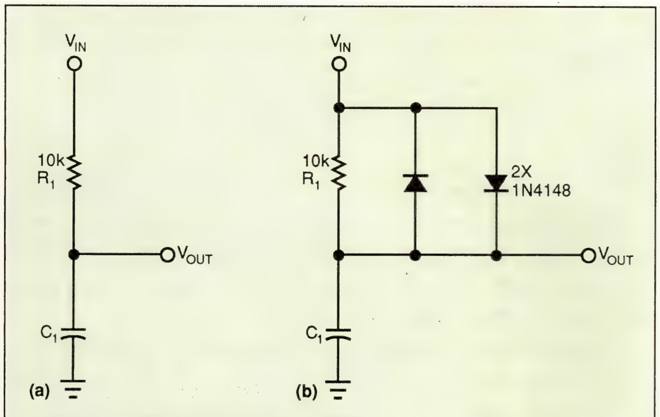
and R_1 are the only active components. At this point, the circuit behaves like a normal, single-pole RC filter.

Assuming that the diode's R_{on} is very small and thus negligible, this filter's improvement in settling time depends on the ratio of the input step and the forward-biased diode's voltage. For a 20V step—−10 to +10V, for example—the filter improves settling time by ln(0.6/20), or 3.5 time constants. In other words, for a 20V step, the simple, diode-clamped nonlinear filter shortens the normal RC filter's 0.01% settling time from 9.2 time constants to $9.2-3.5=5.7$ time constants. However, as the ratio between the input voltage and the diode's forward voltage decreases, so does this circuit's advantages. The settling-time improvement decreases for smaller input steps. When the input step equals the forward-biased diode's voltage drop, the circuit provides no improvement in settling time.

Lower the threshold

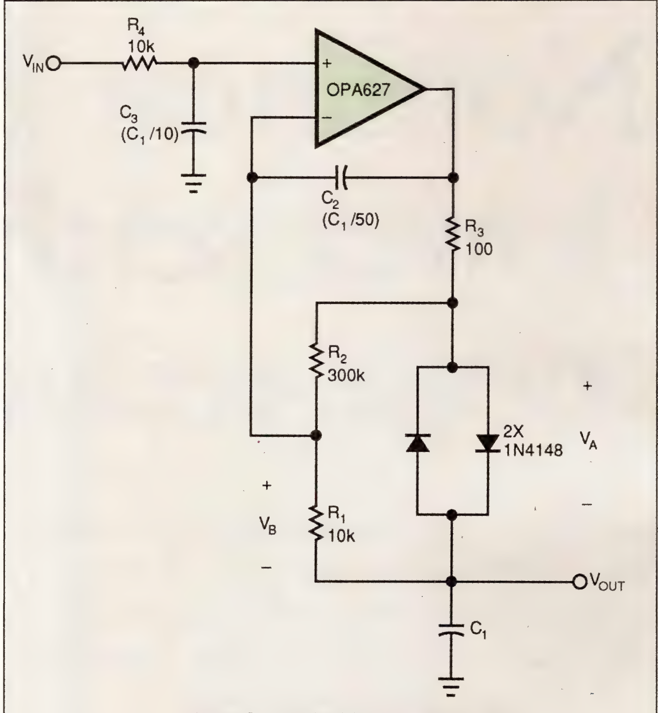
By reducing the threshold to below 0.6V, you can improve the settling time for even smaller inputs. The improved nonlinear filter shown in **Fig 2** lets you adjust the clamp threshold by choosing the values of R_1 and R_2.

Fig 2's op amp forces the voltage at its inverting input to be the same as the signal at the noninverting input. Small voltage differences between the input and the output voltages appear across R_1, because the diodes don't have adequate forward bias and are therefore off. Under these conditions, the filter behaves like a single-pole filter with a time constant determined by the values of R_1 and C_1.



Note: C_1 = 1592 pF FOR 10-kHz FILTER

Fig 1—You can improve the settling time *of the standard RC filter (a) by adding two diodes (b). C_1 charges and discharges much faster through the diode's low on-resistance than it can through R_1, thus improving settling time.*



Note: C_1 = 1592 pF FOR 10-kHz FILTER

Fig 2—To improve settling time *for small inputs as well as large inputs, this circuit allows you to set the noise threshold by choosing the values of R_1 and R_2.*

The voltage divider formed by R_1 and R_2 forces the voltage V_A to equal

$$V_A=V_B[(1+(R_2/R_1)].$$

When the input voltage increases (when you apply a step voltage, for example), V_A increases. When the voltage difference between the input and output approaches $0.6V/(1 + R_2/R_1)$, the diode that corresponds to the input's signal polarity will begin to conduct, and the capacitor will rapidly charge through that diode.

To determine **Fig 2**'s component values, you'll have to consider the noise-reduction requirements of your filter. For example, if you want to filter the noise of a 20V step to 0.01% resolution, you'll also filter the signal's peak noise to less than 0.01% of 20V, or 2-mV peak. A clamp threshold of ten times this peak, or 20 mV, is an arbitrary but ample nonlinear threshold. The component values shown in **Fig 2** set the filter's threshold to 20 mV. The time constant of the filter is very small, regardless of which diode is on, and the settling time is limited only by the op amp's slew rate or current limit. For a 20V step, **Fig 2**'s improvement in settling time is $\ln(0.02/20)=6.9$ time constants. In other words, the improved nonlinear filter can improve the 0.01% settling time of a 20V step from 9.2 time constants to $9.2-6.9$, or 2.3, time constants—a 4-to-1 improvement. Further reducing the 20-mV threshold provides little additional settling-time improvement.

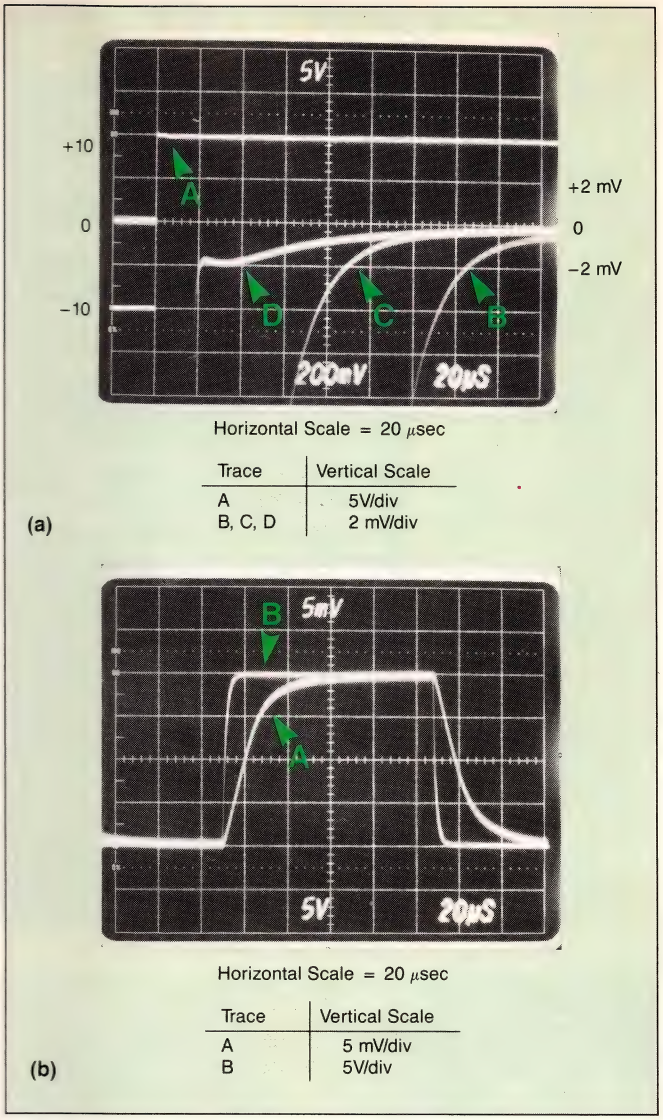
To use this filter successfully, you need to know the noise content of your input signal. If the noise of your signal is greater than the threshold—20 mV in this case—the filter will mistake the noise as a step input and fail to filter it out. Thus, **Fig 2** only behaves like the desired filter for noise signals below the threshold that you set. If the noise exceeds 20 mV, **Fig 2**'s circuit won't behave as an RC filter with the desired 10-kHz cutoff. To prevent this situation, you can ensure that the noise signal at the op amp's input doesn't exceed 20 mV by using C_3 and R_4 to prefilter the input.

To reduce the prefilter's effect on settling time, the values of R_4 and C_3 set the prefilter's bandwidth ten times higher than the bandwidth of the noise filter. At this higher bandwidth, the prefilter's effect on settling time is negligible, and the noise at the prefilter's output is $\sqrt{10}$ times greater than 2 mV, or a little over 6-mV peak. (Recall that noise is proportional to the square root of the bandwidth.) A noise level of 6 mV provides a comfortable margin for a 20-mV threshold.

Choose the right filter ingredients

Op amps tend to become unstable and to oscillate when driving large capacitive loads. The network comprising C_2 and R_3 in **Fig 2** ensures circuit stability when the op amp is driving large values of C_1 through the low impedance of the forward-biased diode network. You may not need this network if C_1 is a small value.

When choosing the op amp for the improved filter, make sure it has enough output-drive capability to charge C_1. Also, the op amp's bandwidth, slew rate, settling time, and dc precision must be adequate for the necessary filter response. Choose an op amp such as the OPA627, which combines dc precision, high slew rate, fast settling time and high output-drive capability. Also, notice that any unity-gain op amp's noise adds noise to the signal. If you choose a low-noise op amp, the op amp's noise contribution is usually negligible. For example, the OPA627 adds only 6% of the 10-kΩ resistor's theoretical minimum noise to the total system noise. Remember that noise adds as the square root of the sum of the squares. Therefore, to determine how much the 4.5 nV/$\sqrt{\text{Hz}}$ noise of the op amp adds to the 12.8 nV/$\sqrt{\text{Hz}}$ noise of the resistor, calculate the square root of the sum of the squares of the combination and compare that to the noise of the resistor alone. In this case, $\sqrt{(4.5)^2+(12.8)^2}/12.8=1.06$, or a 6% increase.



Horizontal Scale = 20 µsec

Trace	Vertical Scale
A	5V/div
B, C, D	2 mV/div

(a)

Horizontal Scale = 20 µsec

Trace	Vertical Scale
A	5 mV/div
B	5V/div

(b)

***Fig 3**—The response of each filter (a) to an input step (trace A) shows the graduated settling-time improvement from the simple RC filter (trace B) to the improved nonlinear filter (trace D). The double-exposure scope photo in (b) contrasts the small-signal (trace A) and large-signal (trace B) settling times of the improved nonlinear filter.*

Fig 3a shows the responses of the standard RC, diode-clamped, and improved nonlinear filters to a −10-to-+10V input step. The bandwidth of each filter is 10 kHz. The measurement circuit adds a gain of 100 between the scope and the circuit, so each horizontal division for traces B, C, and D represents 2 mV, or 0.01% of a 20V step. Thus, the filters settle to within 0.01% when their corresponding traces lie within one division below the center line of the scope.

For a 10-kHz filter, one RC time constant is 15.9 µsec. **Table 1** displays the theoretical settling times of each filter. These tabulated settling times ignore the input slew rate and the diode forward resistance,

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Table 1 — Theoretical time constants and settling times

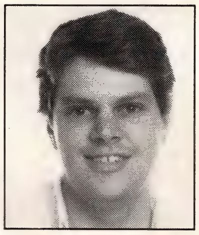
Filter type	Theoretical settling time (time constants)	Theoretical settling time (μsec)*
Single-pole RC	9.2	147
Diode-clamped nonlinear	5.7	91
Improved nonlinear	2.3	37

*Time required to settle within 0.01% of final value for a 10-kHz filter

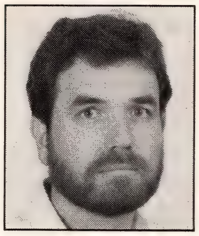
which are good approximations for the OPA627-based, 10-kHz filter. The actual measurements closely match the theoretical calculations.

Fig 3b is a double-exposure scope photo of the improved nonlinear filter operating with a low (trace A) and high (trace B) input signal level. The filter's response to a ±10-mV step looks like the response of a standard, 10-kHz, single-pole RC filter. You'd expect this response, because the input is equal to the threshold voltage. When the circuit operates with a high input level (a ±10V input step), the settling time greatly improves. EDN

Authors' biographies



Rod Burt is a senior engineer at Burr-Brown. Rod designs linear ICs, including precision op amps, instrumentation amplifiers, and isolation amplifiers. He received his BSEE from the University of Arizona.



R Mark Stitt, a senior engineer at Burr-Brown, manages the design of linear ICs, including amplifiers and voltage and current references. He received his BSME from the University of Arizona and holds 13 US patents.

Article Interest Quotient (Circle One)
High 479 Medium 480 Low 481

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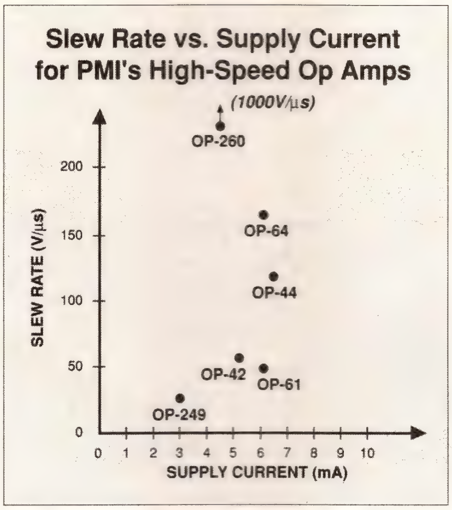

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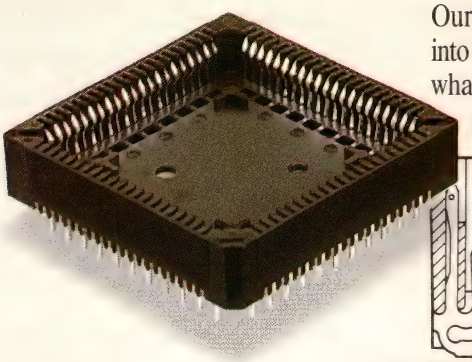

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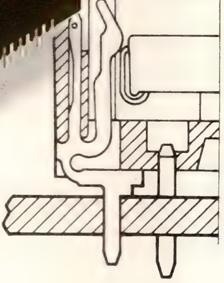

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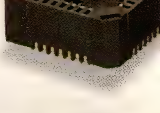
Two basic styles of sockets are available: square or 32-position rectangular EPROM and SO-J. Both come in solder



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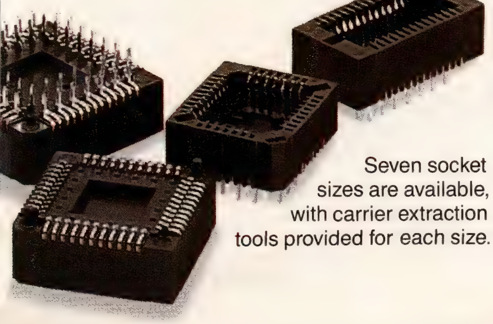
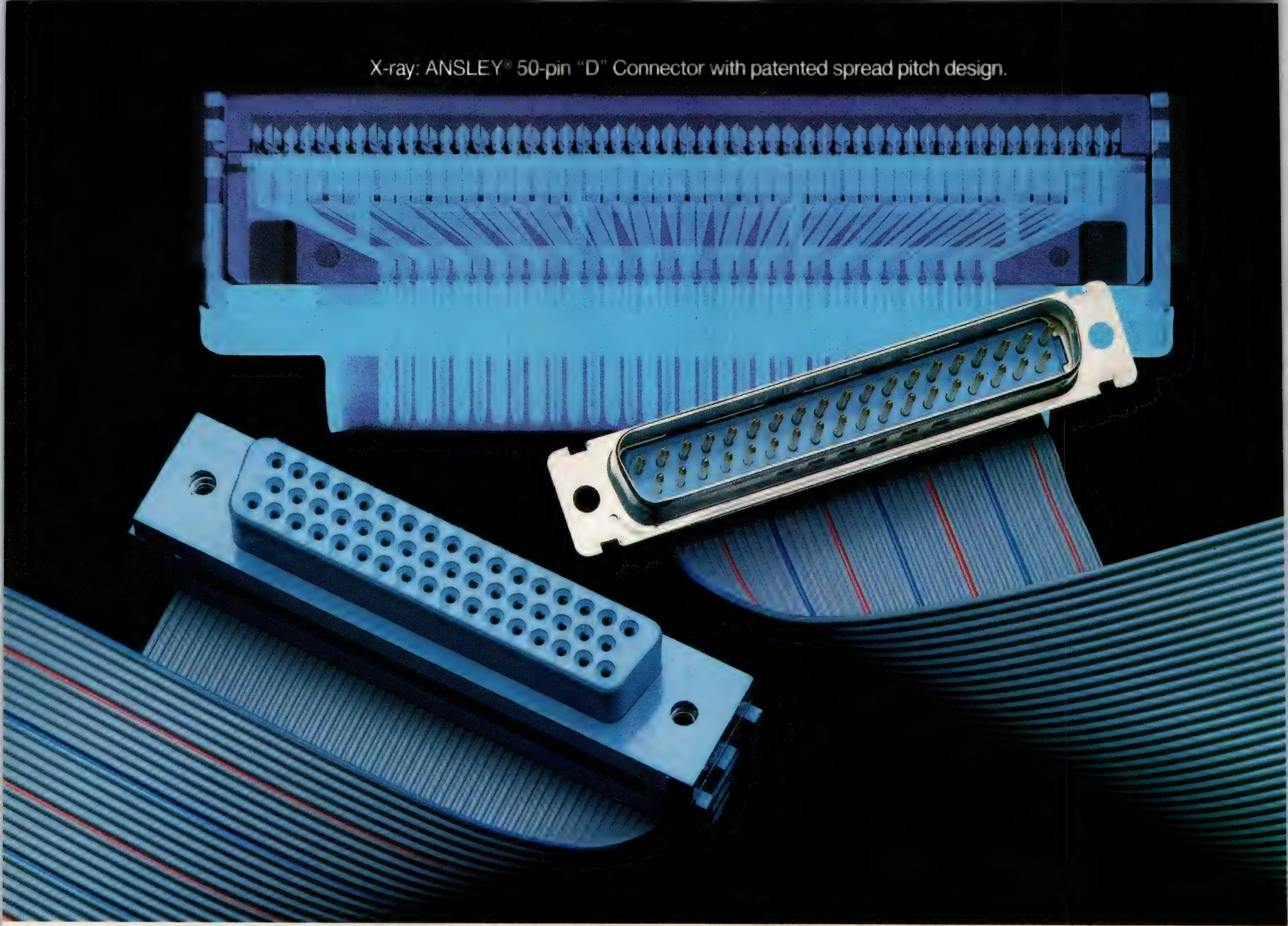


Seven socket sizes are available, with carrier extraction tools provided for each size.

Call the AMP Information Center at 1-800-522-6752 for literature on HPT PLCC Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

CIRCLE NO. 146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DESIGN IDEAS

EDITED BY ANNE WATSON SWAGER

Simple circuit extracts TV sync pulse

Andrew K Dart
Andy's Bureau of Standards, Duncanville, TX

The circuit in **Fig 1** uses a sync-separator chip, a counter, and a decoder to detect the horizontal sync pulse that occurs at the beginning of line 10 in field one of an NTSC television picture. You can use this circuit to compare the time delay between sync signals at various locations, and to determine and correct for any drift between the two master clocks.

The output of the LM1881 sync separator is the key to detecting line 10; the odd/even line goes high on the leading edge of the first equalizing pulse in the middle of line 4. Thus, you can use this knowledge to find virtually any other line in the field. This particular circuit locates line 10 of field one. The circuit resets the 74LS161 counter until the odd/even line goes high. Then, 74LS161 counts the positive transitions of the sync signal. After eleven positive transitions, the sync pulse drives pin 4 of the 74LS138 decoder low, and the line-10 sync pulse appears at pin 12 of the decoder. (The circuit counts to eleven—as opposed to the six you might expect—because the composite sync signal contains more than one pulse per line.) The counter remains in its maximum-count state until the sync separator causes a reset because Q_1 feeds the inverted terminal-count output back to the parallel-enable input.

To Vote For This Design, Circle No. 746

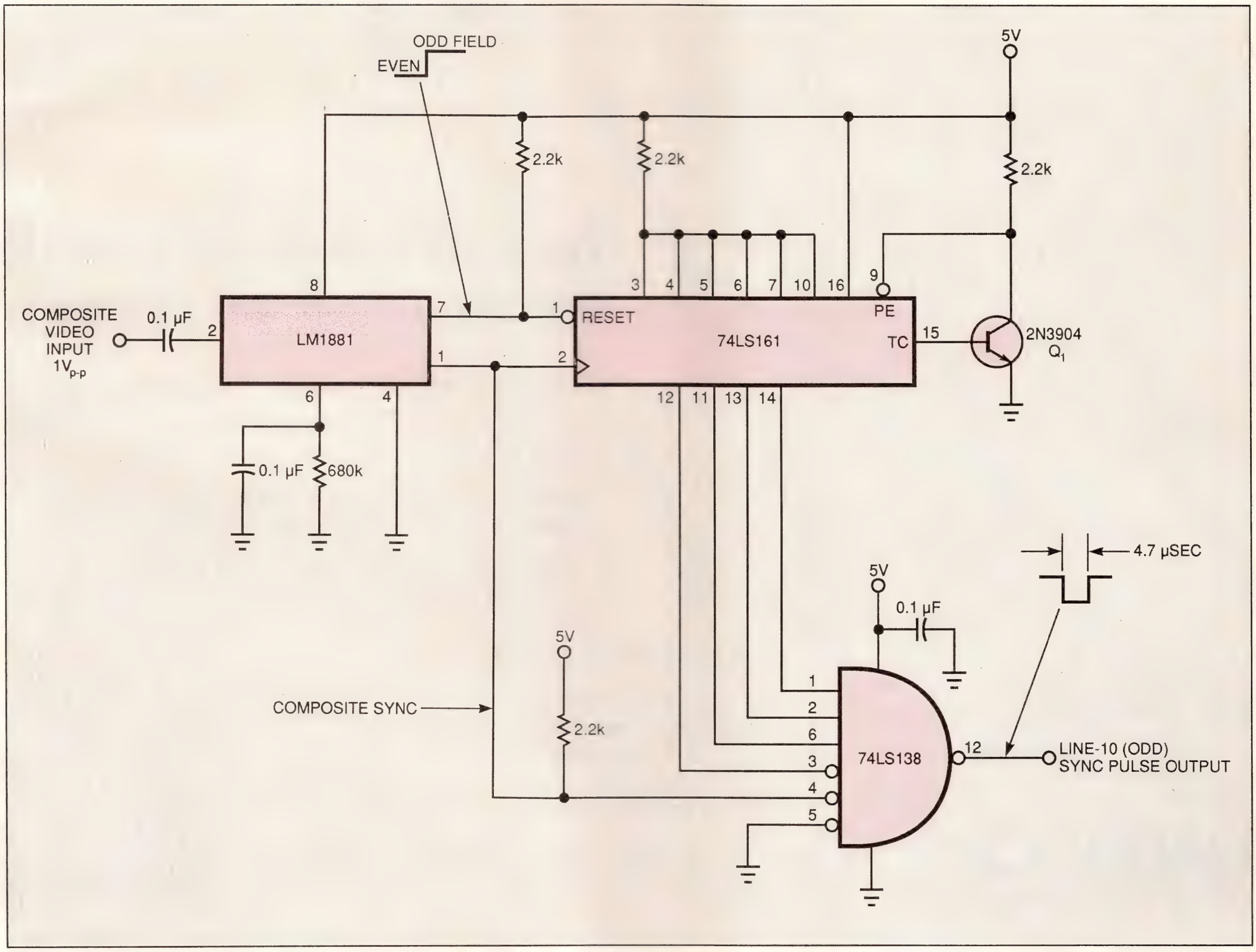

Fig 1—You can take advantage of the sync separator's odd/even field output *to extract the sync pulse at line 10 of a TV signal.*

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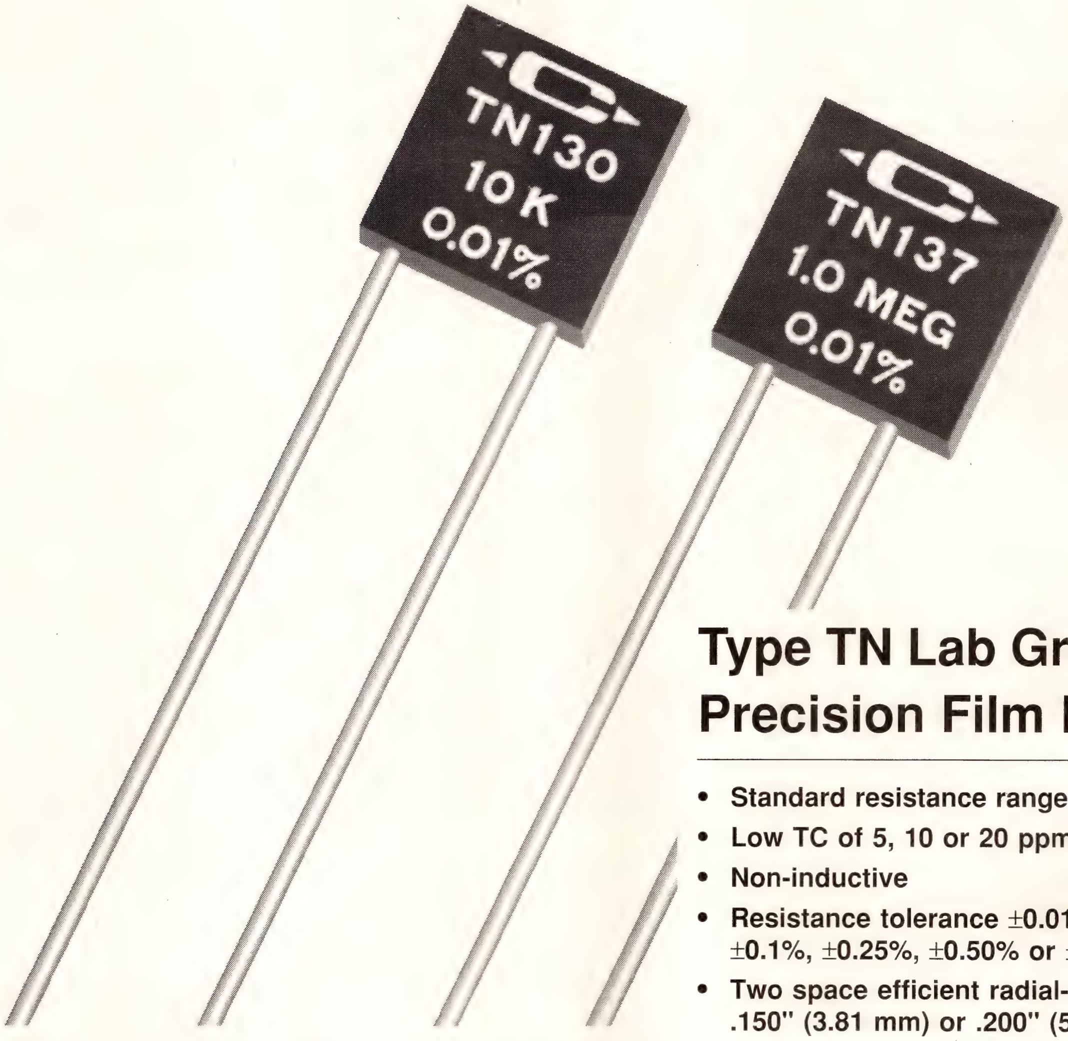

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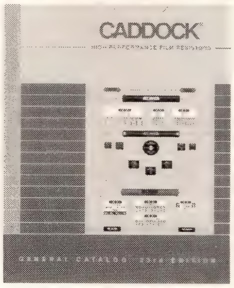

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CIRCLE NO. 113

Voltage-divider switch adds range to DPM

Don Sherman
Maxim, Sunnyvale, CA

You can extend the range of many currently available digital-panel-meter (DPM) chips and modules by adding a voltage divider switch to the DPM's input (**Fig 1**). If you use mechanical switches, the contacts' resistance won't affect the divider's ratio. However, if you use solid-state switches, you need to include the switch resistance in your voltage-divider equations. Unfortunately, an analog switch's exact resistance varies with temperature and the power-supply voltage.

Fig 1's circuit overcomes this problem by using the differential inputs of the DPM to remove the analog switch's IR drop which is in series with the divider resistor. The second analog switch in each pair carries no current. This switch connects the INPUT LO pin to the bottom of the precision voltage-divider resistor, and causes the divider to ignore the voltage drop in the companion, current-carrying switch.

You must supply the analog switch, in this case the DG509A analog multiplexer, with both a positive and negative voltage if you want it to pass positive- and negative-going voltages. **Fig 1** generates the negative voltage using the MAX138's internal charge-pump; the V⁻ pin can supply as much as 0.5 mA. You can build the precision divider with discrete 1% resistors, or purchase a precision resistor network. As **Fig 1** shows, you can control the voltage-divider switch by using a microprocessor and the select pins of the multiplexer. **EDN**

To Vote For This Design, Circle No. 747

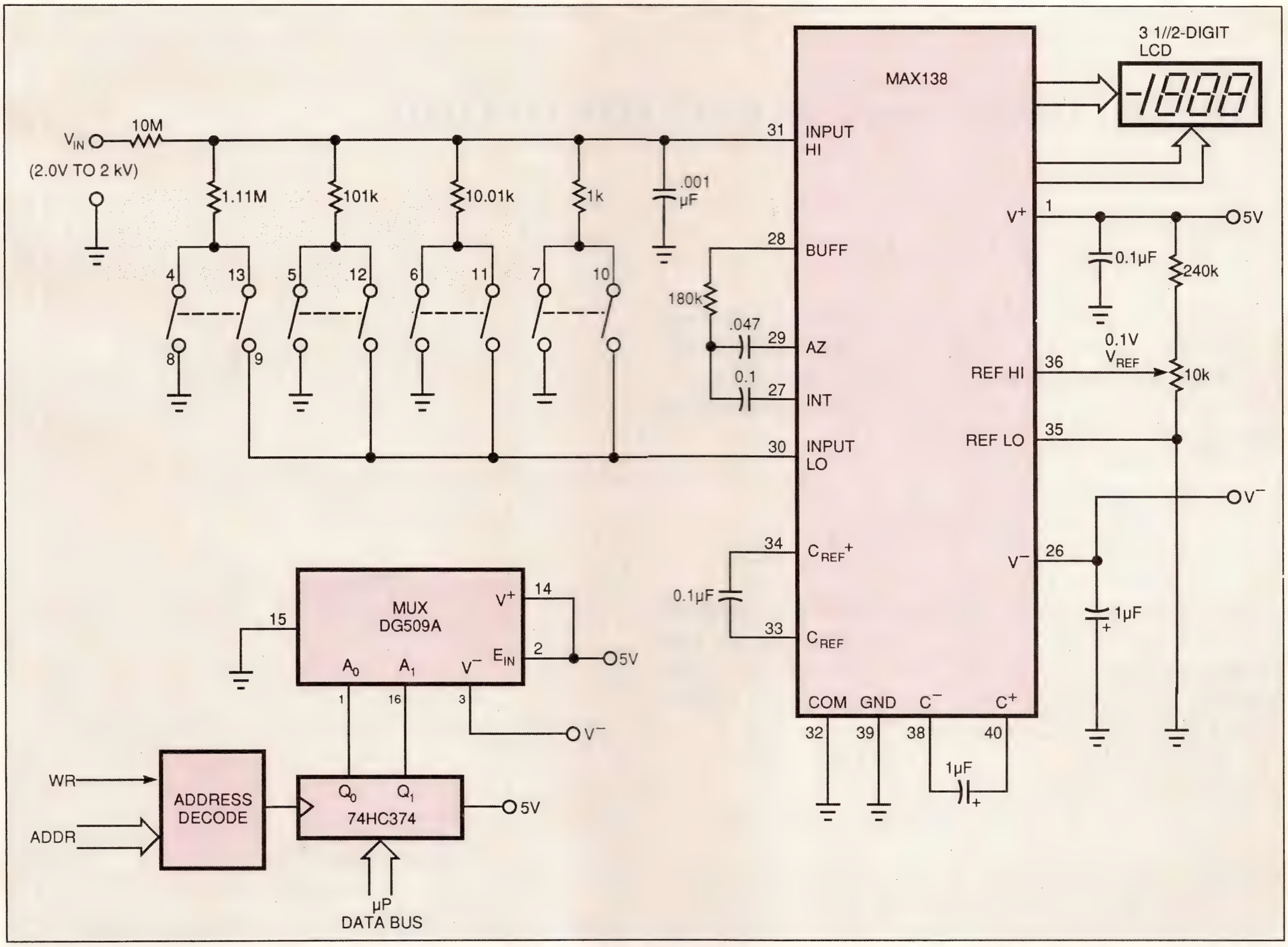

Fig 1—To extend the range of a digital-panel-meter chip or module, *you can add a precision voltage divider to the device's input.*

Infrared imager finds pc-board shorts

John Darjany
Griffin Technology Inc, Compton, CA

By using temperature-sensitive liquid-crystal sheets, you can implement a type of low-cost infrared imaging system that easily locates shorts on bare pc boards. First, you connect a dc power supply to your board's shorted nodes. You may need to add a series resistor to set the current to a fairly high level compared to the trace size. For example, you may want small traces to carry 100 mA, and large traces to carry 2A. You may also need to adjust the power-supply current to achieve useful results.

To find the short, lay the sheets on the bare board, making sure to make good contact with the board's surface. The heat generated by the short will create an image on the sheet. If the image isn't initally clear, the problem may be on the other side of the board. Simply turn it over and repeat the process. The sheets come in different temperature ranges and work quite well in a typical air-conditioned building with a temperature around 25 to 30°C. One source for the sheets is Edmond Scientific (Barrington, NJ).

To Vote For This Design, Circle No. 748

Digital filter speeds execution time

George Ellis
Industrial Drives, Radford, VA

The filter that corresponds to the block diagram in **Fig 1a** improves upon two simpler digital filters by providing unity dc gain and faster execution time. The simplest transfer function of a single-pole lowpass digital filter is

$$\frac{\mathrm{OUT}}{\mathrm{IN}}(z)=\frac{z}{z-e^{-\omega T}}=\frac{1}{1-e^{-\omega T}\,z^{-1}}.$$

This filter, for which **Fig 1b** is one block-diagram implementation, has one major limitation: the dc gain is greater than one. By adding a gain term to the transfer function as follows, you can create a filter with a dc gain of unity **(Fig 1c)**:

$$\frac{\mathrm{OUT}}{\mathrm{IN}}(z)=\frac{1-e^{-\omega T}}{1-e^{-\omega T}\,z^{-1}}.$$

Unfortunately, this filter also has limitations because it requires two multiplications, which slow execution time and increase the round-off error. You can eliminate these problems by rearranging the denominator

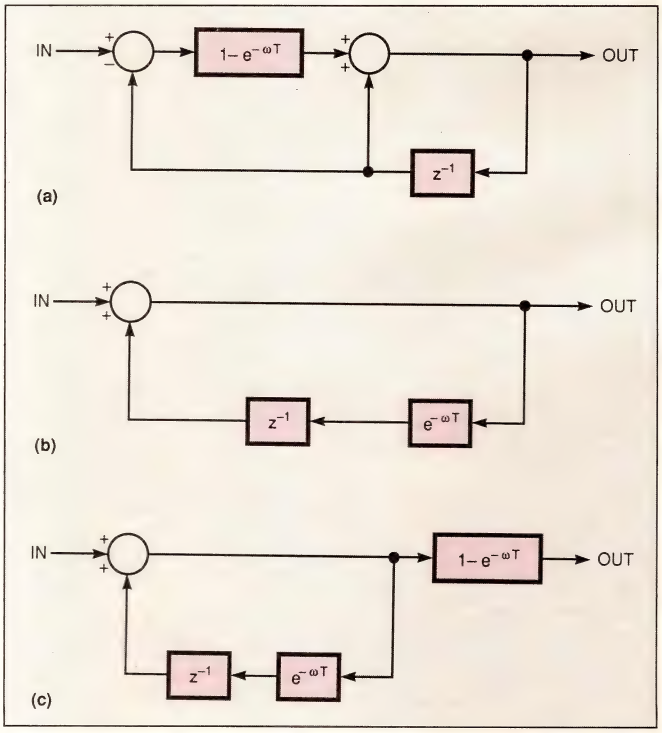

***Fig 1—The improved digital filter (a)** features unity dc gain unlike the simple filter in **b**, and requires only one multiplication unlike the filter in **c**.*

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100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ. 1.3	max. 1.6	typ. 1.3	max. 1.6
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F126 REV.A

of the transfer function to equal

$$\frac{OUT}{IN}(z)=\frac{1-e^{-\omega T}}{1-z^{-1}+(1-e^{-\omega T})\,z^{-1}}.$$

A block diagram of this filter **(Fig 1a)** shows that the filter only requires one multiplication. Also, the range of all intermediate variables is less than the range of the input. This last feature is important when the input range is close to the size of the word. If the input value is close to the limit of the filter's word size (for example, ±32767 for 16 bits), and the intermediate variables have a range larger than the input (as is the case with the first two filters), the intermediate variables must have extended precision to prevent overflow. Extending the precision causes an increase in execution time.

You can implement **Fig 1a**'s filter with the one-line algorithm

$$OUT_n=(IN_n-OUT_{n-1})(1-e^{-\omega T})+OUT_{n-1},$$

where OUT_n is the new output, OUT_{n-1} is the output from the previous cycle, IN_n is the new input, ω is the filter's bandwidth in rad/sec, and T is the system sample time ($e^{\omega T}$ is a constant).

To Vote For This Design, Circle No. 749

Magnetic fields tune oscillator

Brian Kormanyos
University of Washington, Seattle, WA

Fig 1 is a familiar variable-frequency oscillator with a twist: current through an electromagnet generates a magnetic field which varies the inductance. This current-variable inductor allows you to design controlled oscillators without using varactor diodes or mixers.

The toroidal inductor has the following value when I_{CTRL} is zero:

$$L=\frac{0.4\pi\mu N^2A\times10^{-8}}{l},$$

where μ is the core permeability, N is the number of turns, A is the core's cross section in cm^2, and l is the core's magnetic path length in cm. As I_{CTRL} increases, the toroidal core moves toward saturation because of

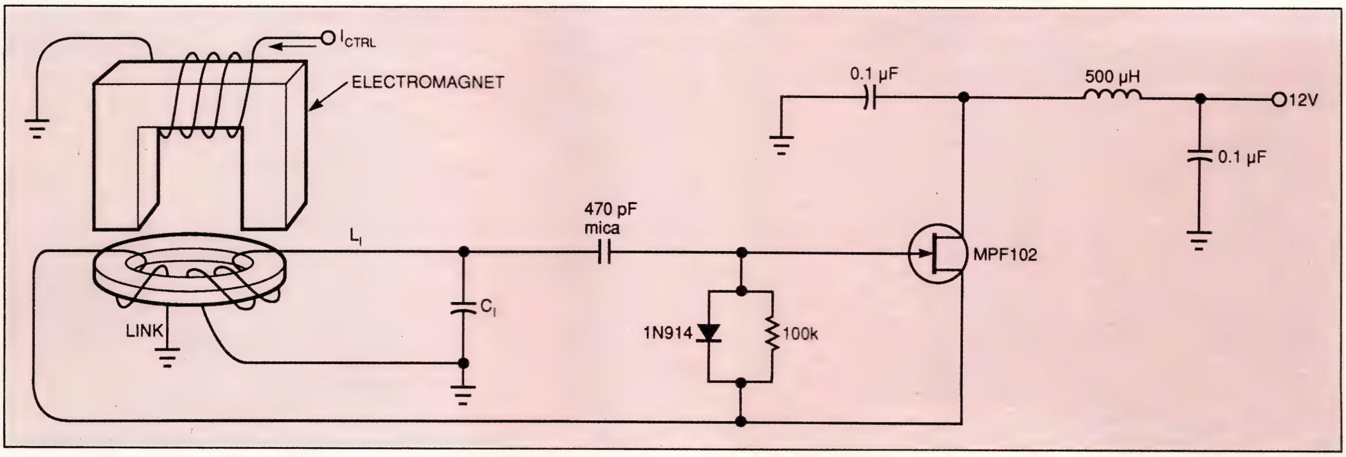

Fig 1—This current-controlled variable inductor *is an alternative to mixers and varactors;* I_{CTRL} *generates magnetic fields that vary the inductance and thus tune the oscillator.*

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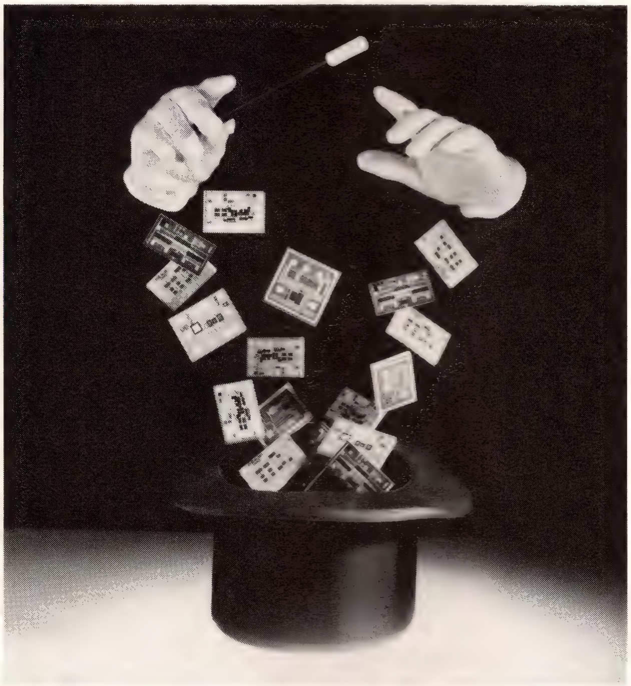

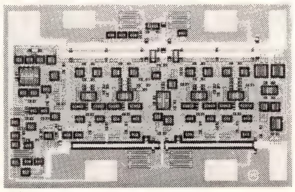

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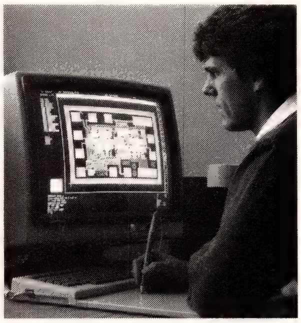

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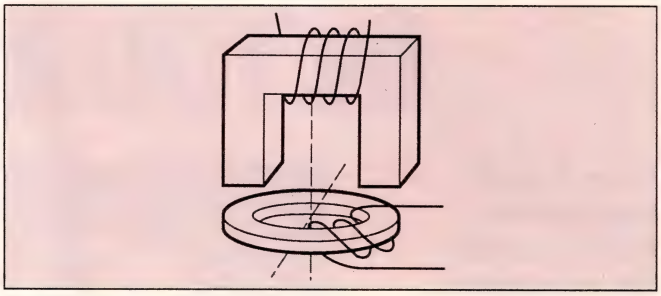

***Fig 2—The optimum position** of the magnet and toroid is the 90° relationship shown.*

the external field generated by I_{CTRL} and the electromagnet. The deviations from linear core behavior amount to a change in core permeability according to the equation, $B=\mu H$. The permeability of the core decreases toward its free space value, and the inductance decreases because it is directly proportional to μ. The frequency then increases according to the equation

$$\omega=\frac{1}{\sqrt{L_1 C_1}}.$$

The separate toroidal core and electromagnet structures ensure that the alternating fields in the toroid have very little coupling to the electromagnet. Thus, the fields are unaffected by low impedance sources for I_{CTRL}. **Fig 2** shows the optimum position of the magnet and toroid. The electromagnet must provide a strong field, and the toroidal core should have high permeability and a gradual saturation characteristic. Many ferrite toroids exhibit these characteristics.

Fig 1's output is sinusoidal and has a frequency range of 500 kHz to 5 MHz. The circuit featured this frequency range with 14 turns for L_1 and 3 turns for the link. The link should always have fewer turns than L_1 to ensure enough voltage gain to sustain oscillation. Your circuit's particular operating frequency depends on the value you choose for C_1 and the nominal inductance of L_1. One limitation of this circuit is that the value of I_{CTRL} can be excessive depending on your magnet design and core material. Also, the relationship between the frequency and current is very nonlinear.

To Vote For This Design, Circle No. 750

LINEAR TECHNOLOGY

DESIGN NOTES

Number 31 in a series from Linear Technology Corporation *February, 1990*

Isolated Power Supplies for Local Area Networks

Sean Gold

Introduction

Local Area Networks such as Ethernet™ or Cheapernet™, require low cost isolated power supplies with modest line and load regulation. Table 1 summarizes the objective design specifications based on IEEE 802.3 and ECMA 200-V. The LT1072 high efficiency switching regulator can be used in isolated flyback mode to satisfy these requirements with minimal support circuitry.[1]

Table 1. Power Supply Specifications for Figure 1

PARAMETER	VALUE	COMMENTS
V_{OUT}	–9V	Ethernet $11.4V < V_{IN} < 12.6V$ Cheapernet $4.55V < V_{IN} < 5.45V$
Ripple	$V_n < 10mVp\text{-}p$	
I_{LOAD}	150mA	40mA Min, 250mA Max
Load Reg	5%	
Line Reg	5%	
Efficiency	e>70%	
Isolation	3000V 500V	Ethernet Cheapernet

Circuit Design

Figure 1 illustrates the design approach. In isolated flyback mode, the LT1072 has no electrical connection to the load; instead, the regulator obtains a feedback signal from the transformers flyback voltage during the switch off-time. The voltage sense occurs after a 1.5μs delay, which prevents the internal error amplifier from regulating the voltage spike due to transformer leakage inductance. The LT1072 compares the feedback signal with a reference voltage, which is set at the feedback pin with a resistor to ground. The primary voltage is regulated to $16V + (V_{FB}/R_{FB})7k$. The feedback pin voltage V_{FB}, clamps to about 400mV, and the term $(V_{FB}/R_{FB})7k$ is nominally set to 2V, making the total flyback voltage 18V. The circuit is programmed for –9V output by setting the transformer turns ratio to 2 to 1. The feedback resistor R_{FB}, includes a 500Ω trim to take into account variations in the clamp voltage and gain within the LT1072.

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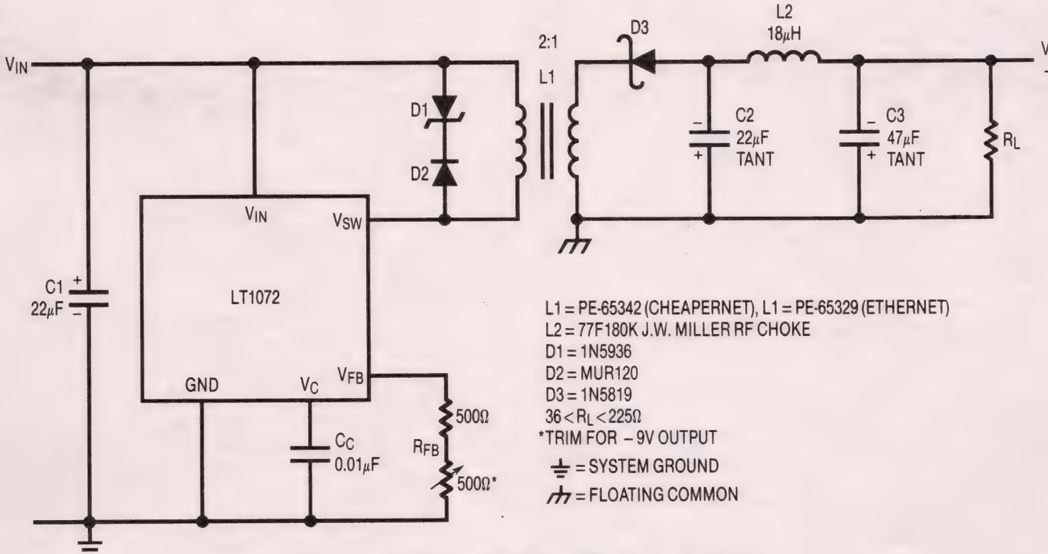
[1] **Note 1:** LTC's Application Note 19, the LT1070 Design Manual, presents a detailed discussion of isolated flyback mode and general information on switching regulator design.



L1 = PE-65342 (CHEAPERNET), L1 = PE-65329 (ETHERNET)
L2 = 77F180K J.W. MILLER RF CHOKE
D1 = 1N5936
D2 = MUR120
D3 = 1N5819
$36 < R_L < 225Ω$
*TRIM FOR –9V OUTPUT
⏚ = SYSTEM GROUND
⏚ = FLOATING COMMON

Figure 1. Isolated Switching Regulator for LAN

A snubber network consisting of a fast turn-on, high breakdown diode and a 36V Zener diode, limits the magnitude of the leakage inductance spike. This snubber configuration improves efficiency because it minimizes the duration of the inductance spike. A Schottky diode in the secondary reduces the voltage loss to the output and increases efficiency.

Specifications for power supply filters are application dependent. When noise levels of 150mV are tolerable, a single 100μF tantalum capacitor is a suitable supply filter. When output noise below 10mV is required, the use of large output capacitors is often impractical. An LC filter is an appropriate recourse. The optional LC filter in Figure 1 contains an RF choke L2, and tantalum filter capacitors C1 and C2. These components have low effective series resistance (ESR) which helps maintain 5% load regulation.

Figure 2 shows the voltage on the switch pin, trace A, and the current flowing through the inductor, trace B. Trace C is a magnified view of trace A, which more clearly shows regulation of the primary voltage after the switch off-time. Figure 3 shows the voltage and current noise at the output.

Transformer Design

The circuit design for 12V to −9V (Ethernet) and 5V to −9V (Cheapernet) circuits are identical except for the transformer specifications. Both circuits develop a regulated 18V primary voltage, but the available input voltage determines the required primary inductance.

$$L_{PRI} = \frac{V_{IN}}{(\Delta I)(f)(1 + V_{IN}/V_{PRI})}$$

$$= \frac{5V}{(0.3A)(40kHz)(1 + 5/18)}$$

$$= 326\mu H \text{ (Minimum)}$$

Where,

ΔI = Magnetizing Current
f = Switching Frequency
V_{IN} = Input Voltage
V_{PRI} = Primary Voltage

Ethernet requires a larger primary inductance than Cheapernet, which implies a larger transformer. Increased isolation also mandates a larger core to accommodate additional insulation. The transformers used in both applications are shown in Figure 4. The PE-65329 for Ethernet (right) achieves 3700V isolation, while the PE-65342 for Cheapernet (left) provides 500V isolation.[2] These transformers are constructed with low loss core material and low resistance wire, to further improve efficiency.

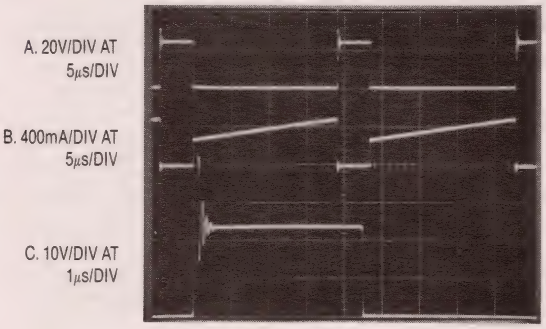


Figure 2. Switching Waveforms

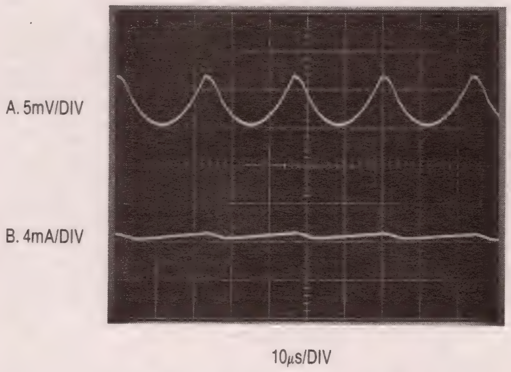


Figure 3. Voltage and Current Noise

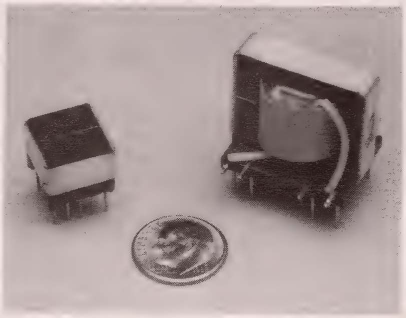


Figure 4. LAN Transformers. PE-65342 (Left), PE-65329 (Right)

For additional literature on switching regulators, call **(800) 637-5545.** For applications help, call (408) 432-1900, Ext. 445.

---

[2] **Note 2:** A 500V version of the Ethernet transformer (PE-65330) is available in the 0.5 inch package in Figure 4.

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IM/GP 1289 165K

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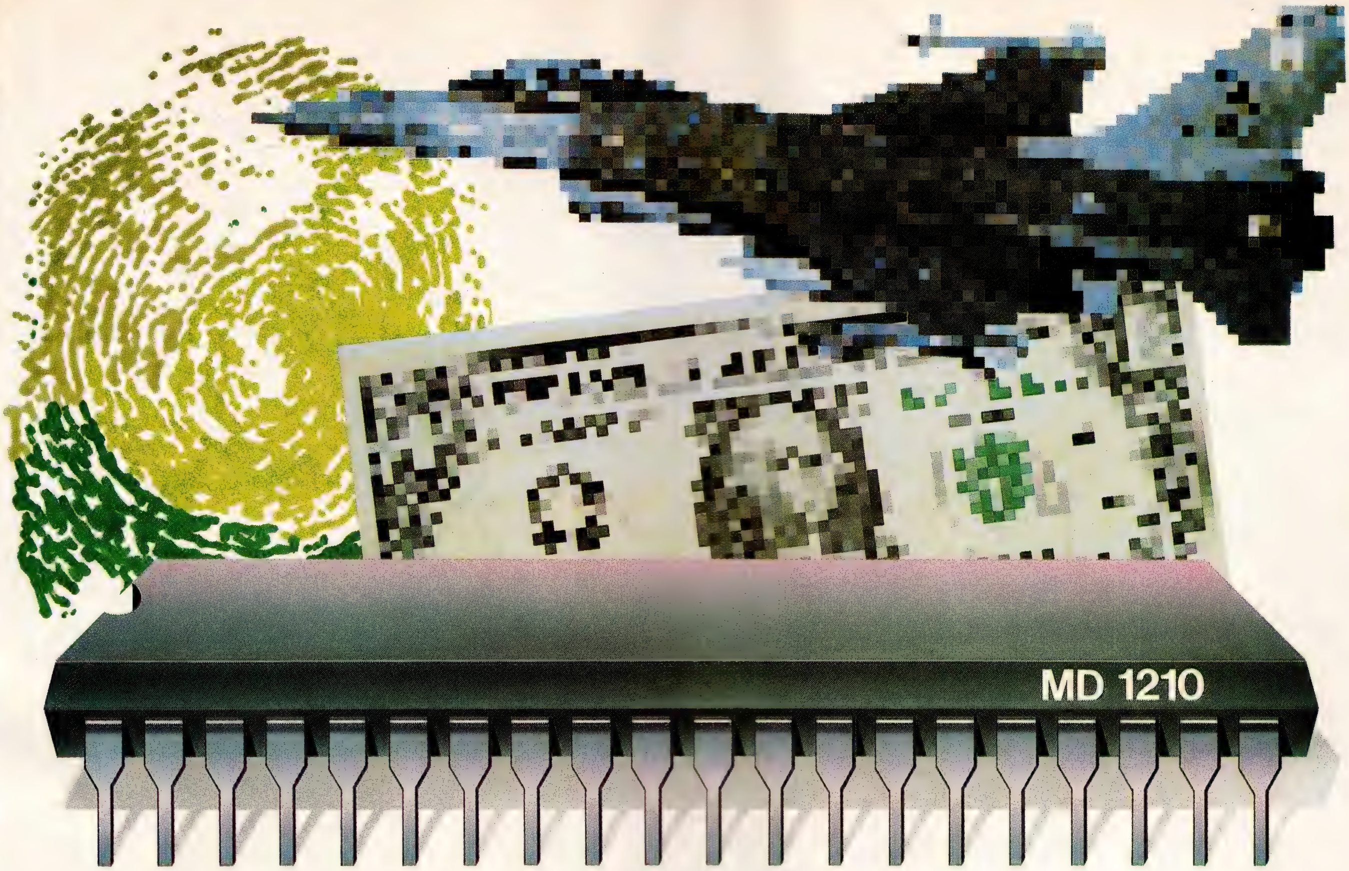

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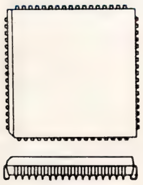
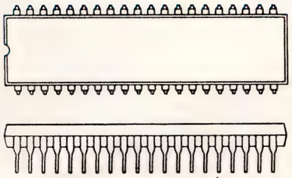

MD1210-1 (68-pin PLCC)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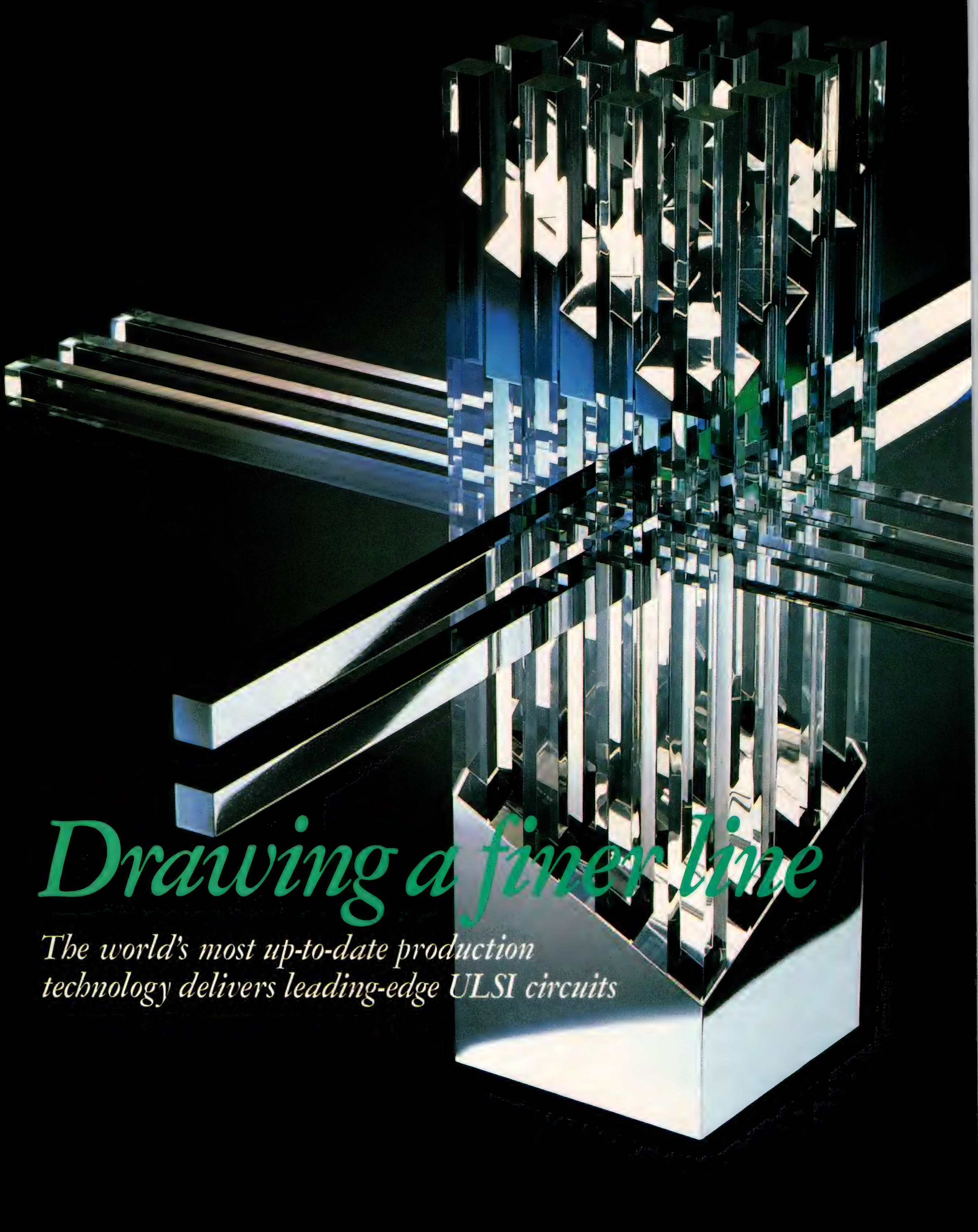

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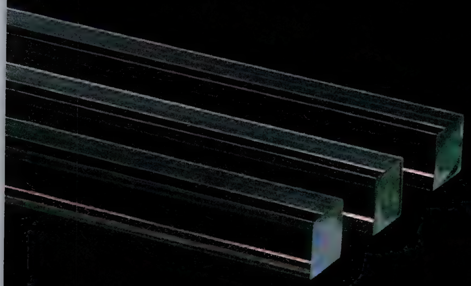

Sub-micron production in full swing, bringing the new age of 4M DRAMs

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CIRCLE NO. 117

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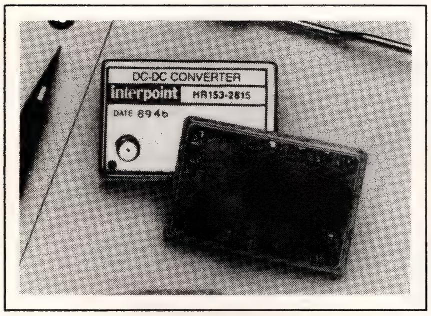
Methode Electronics Inc, Connector Div, 7447 W Wilson Ave, Chicago, IL 60656. Phone (708) 867-9600. **Circle No. 351**



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HR150 Series dc/dc converters have an output capability of 15 to 20W and are available in single-, dual-, and triple-output versions. They accept inputs of 18 to 36V and output 5, ±12, and ±15V. Line and load regulation equal 0.2%, and efficiency measures approximately 80%. The units are housed in metal, hermetically sealed packages, which take 2.4 in.^{2} of board area and measure only 0.5 in. high. Manufactured to MIL-STD-883, the converters have a power density of 12.5 W/in.^{3} and operate over a −20 to +70°C range. $128 (100).

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- *Have 650V-ac isolation*

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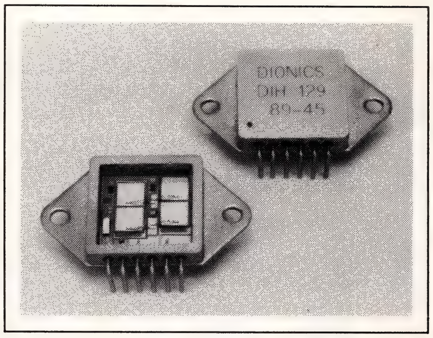

Dionics Inc, 65 Rushmore St, Westbury, NY 11590. Phone (516) 997-7474. FAX 516-997-7479. **Circle No. 354**

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- *Operate over the full military range*
- *Suitable for pc-board mounting*

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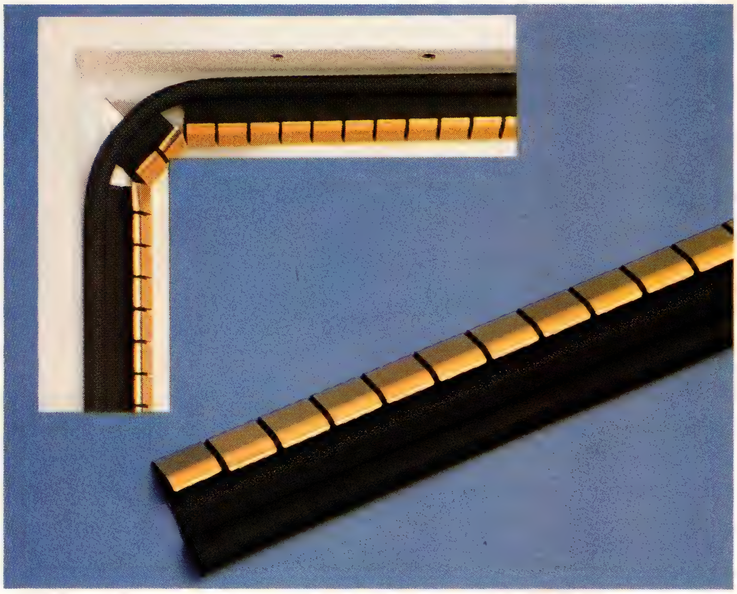

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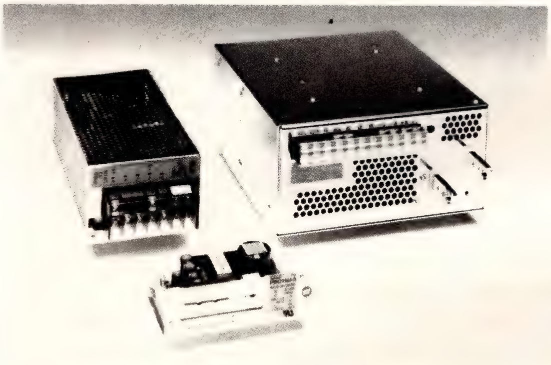

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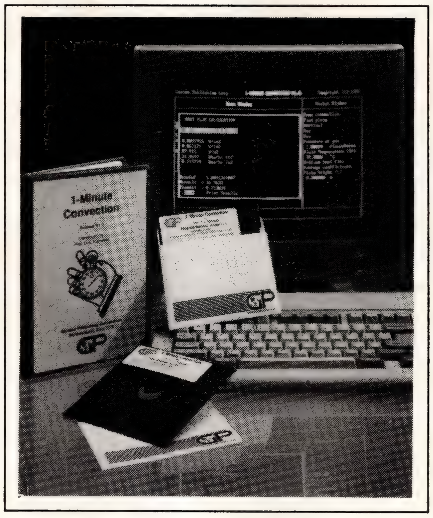

Genium Publishing Corp, 1145 Catalyn St, Schenectady, NY 12303. Phone (518) 377-8854. FAX 518-377-1891. **Circle No. 376**

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OrCAD Systems Corp, Inquiries Manager, 3175 NW Aloclek Dr, Hillsboro, OR 97124. Phone (503) 690-9881. FAX 503-690-9891.
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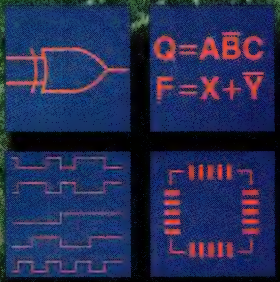

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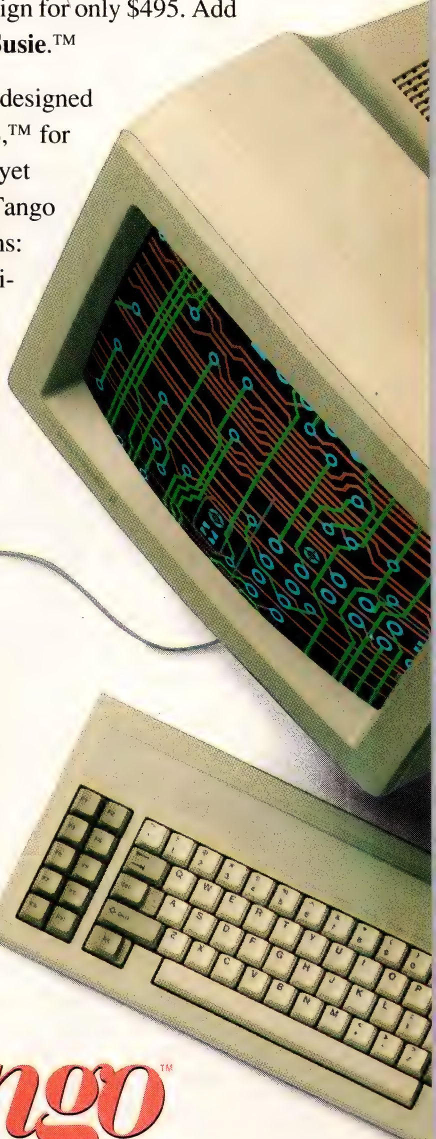

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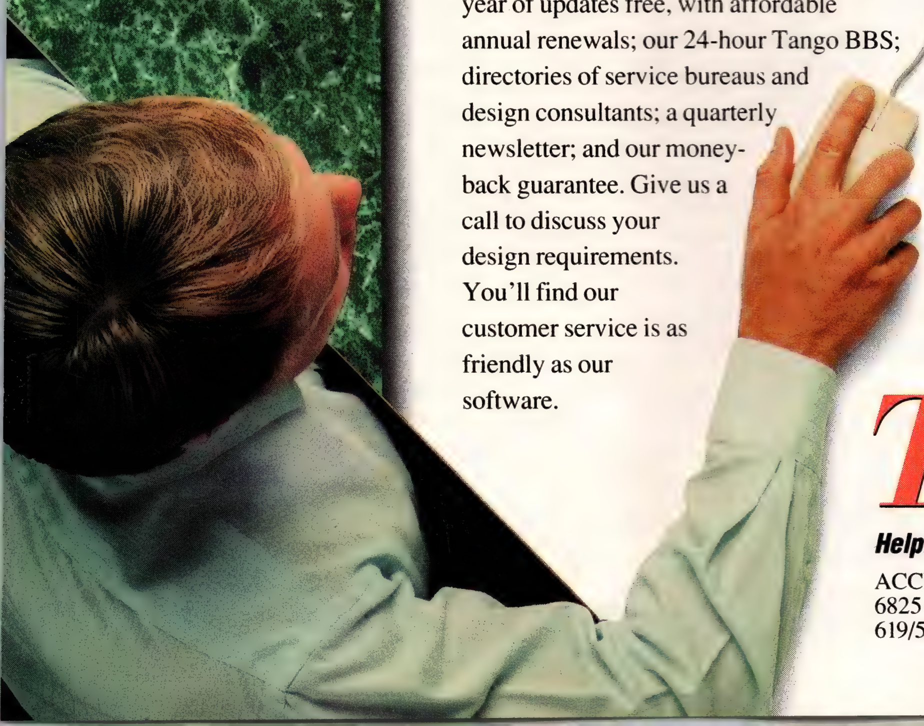

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- *Runs under the OS/2 operating system*

GammaFax Command Language (GCL) and GammaFax Programmer's Interface (GPI) can help you develop communications subsystems that incorporate PC-to-fax features and run under the OS/2 operating system. GCL is a dBase-like command-language interface intended for database applications. GPI is intended for C programmers who are developing applications with fax capabilities. Both tools provide access to all conversion, print, and display routines supplied for use with the vendor's GammaFax board. The GPI package includes specialized support from the vendor's technical-support and engineering departments. $2500/year.

GammaLink, 2452 Embarcadero Way, Palo Alto, CA 94303. Phone (415) 856-7421. FAX 415-494-7042. **Circle No. 379**

Communications Software For HP New Wave

- *Provides pull-down menus and multiple windows*
- *Can act as multiple servers and clients simultaneously*

The DynaComm 2.1 asynchronous-communications software package provides transparent communications between multiple PCs, minicomputers, and mainframes, making use of Hewlett-Packard's New Wave graphical system. The package includes Director, a communications manager that performs all the functions of a phone dialer and lets you execute scripts for logging on to a remote computer. Multichannel dynamic-data-exchange (DDE) capabilities let the program act as multiple servers and multiple clients simultaneously. Using the graphical features of New Wave, the program provides pull-down menus and multiple overlapping windows for multitasking operations. The program complies with the Common User Access (CUA) recommendations of IBM's System Application Architecture (SAA). $295.

Future Soft Engineering Inc, 1001 S Dairy Ashford, Suite 203, Houston, TX 77077. Phone (713) 496-9400. **Circle No. 380**

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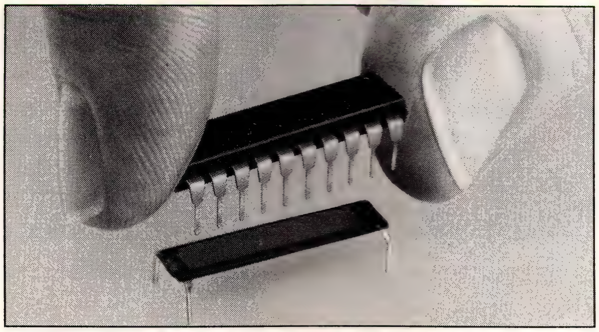
CIRCLE NO. 35

KILL THE NOISE WITH



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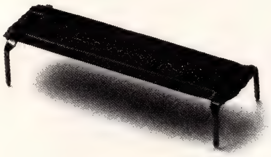
CIRCLE NO. 107

MICRO/Q 1000 STANDARD CAPACITORS

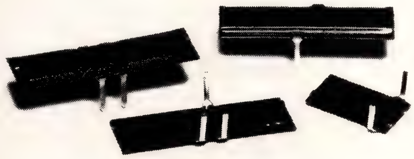
Improve board performance without redesign. Noise problems are solved by retrofitting on existing boards.



CIRCLE NO. 108

MICRO/Q 1000 CUSTOM CAPACITORS

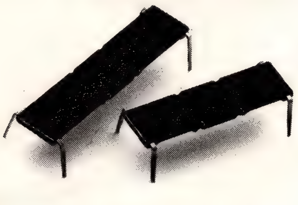
Special pinouts are available to address the wide variety of specialty DIPs such as analog devices, op-amps, and the center pinout advanced CMOS devices. Applications include: decoupling, EMI/RFI filtering, and compensation.



CIRCLE NO. 109

MICRO/Q 2000 CAPACITORS

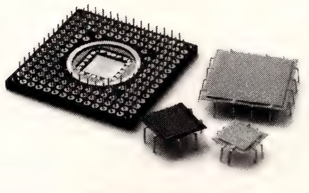
Capacitance levels from 0.01 μF to 0.3 μF in Z5V and X7R temperature stable dielectrics. The unique molded construction provides for maximum environmental protection. Suitable for use in both commercial and military applications.



CIRCLE NO. 110

MICRO/Q 3000 CAPACITORS

Reduces noise associated with the use of PGA and PLCC devices. Several part sizes are available to address a variety of package sizes, Micro/Q 3000 is designed to be used with all 16/32-bit MPUs, DSPs, GSPs, FPPs, gate arrays, standard cells, and fully custom ASICs.



CIRCLE NO. 111

SAY GOODBYE TO WAIT STATES

Now there's an E^2PROM that can keep up with your processor. And, cut your wait states from three or four to one or none.

Atmel. The fastest E^2s in the land. But, maybe blazing speed isn't enough. Well:

HOW ABOUT RELIABILITY? None better. Built-in error detection and correction as well as write protection. All processed to Military Standard 883. We give your system the competitive edge.

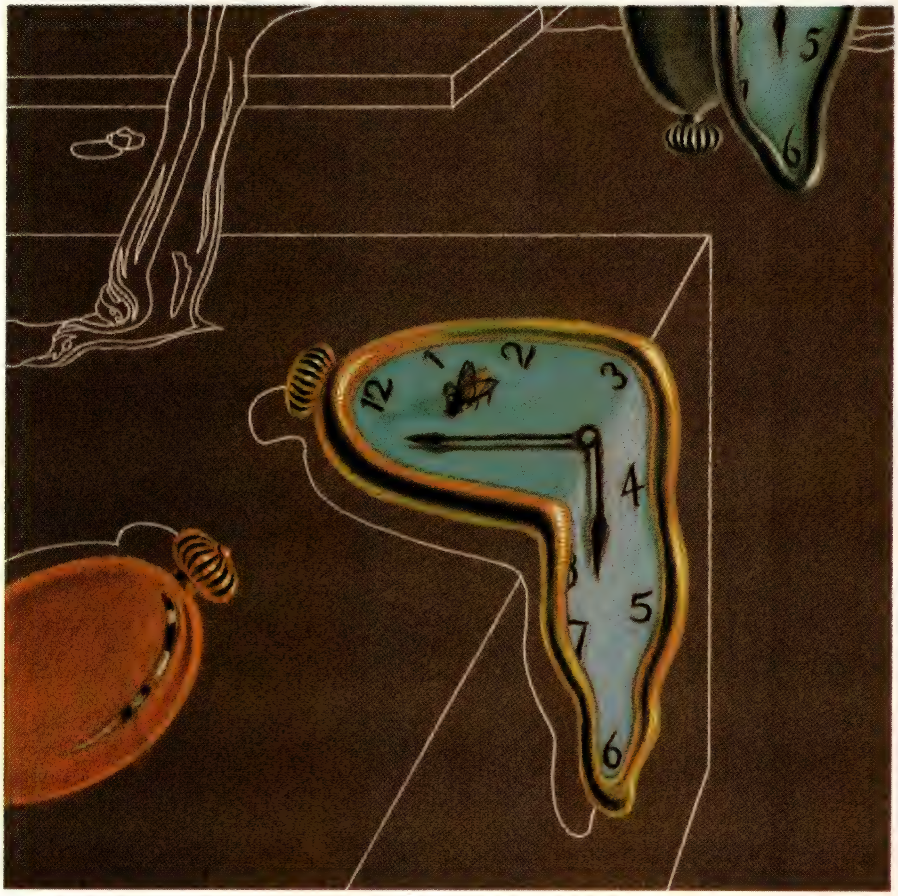
HOW ABOUT POWER? None lower. Perfect for in-flight operations and battery back-up systems.

HOW ABOUT EXTRA FEATURES? We've got them all. Fast write. Page mode. Extended endurance. Software data protection. Chip erase. Package variety. These are just some of the details listed in our data pack. Just ask, and we'll send you one.

So, say goodbye to wait states. And, plug Atmel's performance, quality and versatility into your system.

Device	*Part No.*	*Speed (ns)*	*Power (mA) (active/standby)*
16K	AT28HC16	45-120	80/0.1
64K	AT28HC64	55-120	80/0.1
256K	AT28HC256	70-120	80/0.2
Megabit	AT28MC010	120-350	100/0.3

A partial listing of Atmel's E^2PROMs.



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CIRCLE NO. 147

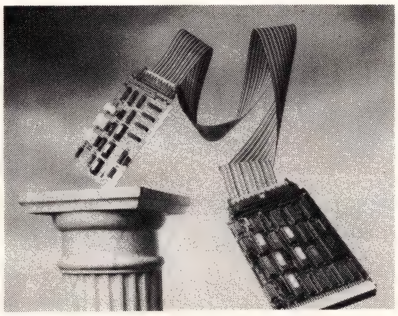
COMPUTERS & PERIPHERALS

Multibus I CPU Board

- *Contains 20-MHz 80386 μP and SCSI port*
- *Also has two RS-232C ports and two iSBX connectors*

The iSBC 386/12S CPU board features a 20-MHz 80386 μP for Multibus I. The board has a SCSI port that lets you eliminate a peripheral controller board. The SCSI controller handles synchronous data rates of 5M bytes/sec and asynchronous data rates of 2M bytes/sec. A FIFO memory buffers the SCSI data. In addition, the board contains two RS-232C ports, a parallel port, two iSBX connectors, a DMA controller, and an iLBX connector. You have a selection of 1M, 2M, 4M, or 8M bytes of RAM and an option for an 80387 coprocessor chip. 1M-byte version, $4900; additional memory, $250/M byte.

Intel Corp, Literature Dept #AP-52, Box 58065, Santa Clara, CA 95051. Phone (800) 548-4725. **Circle No. 356**



ISA Bus-To-STE Bridge

- *Maps STE Bus memory into unused ISA addresses*
- *Each bus's board communicates via a ribbon cable*

The PC-Link is an ISA bus-to-STE Bus bridge consisting of an expansion board for each bus. The boards communicate through a ribbon cable that can be as long as 50 ft. The combination gives an ISA bus computer access to the STE Bus memory and I/O locations. STE Bus memory and I/O addresses map into unused areas in the ISA bus address range. The link gives the ISA bus computer access to STE Bus I/O and signal-conditioning modules. In addition, the link lets an STE Bus computer take advantage of the industrial control software available for the IBM PC computer. Data transfers between the two buses are transparent to the respective host CPUs if the data block lengths are <8k bytes. £495.

Arcom Control Systems Ltd, Unit 8, Clifton Rd, Cambridge CB1 4WH, UK. Phone (0223) 411200. FAX 0223-410457. **Circle No. 357**

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CIRCLE NO. 36

Cartridge-Tape-Drive Controller Boards

- *Data-compression algorithm in hardware*
- *Compatible with the QIC-40, QIC-80, and QIC-150 formats*

The Turbo-Compression boards consist of two cartridge-tape controller boards for the 16-bit ISA bus. Both boards use the StacPack data-compression algorithm from Stac Inc (Pasadena, CA). The algorithm is located in an ASIC in order to increase the data-transfer rate to and from ¼-in. tape drives. The TC-15 is compatible with the QIC-40 and QIC-80 tape formats. When using extended-length ¼-in. tapes, the algorithm expands the capacity of the QIC-40-and QIC-80-compatible tapes to 120M and 250M bytes, respectively. Benchmark tests on a 33-MHz 80386 computer show the backup speed for QIC-40 tape drives increases from 2.3M bytes/minute to 4.5M bytes/minute. The TC-02 is compatible with QIC-150 tape drives and increases the drives' capacity to 500M bytes using extended-length tapes. Benchmark tests show a backup-speed increase from 4.5M bytes/minute to 8.2M bytes/minute. Each board, $399.

Colorado Memory Systems Inc, 800 S Taft Ave, Loveland, CO 80537. Phone (303) 669-8000. FAX 303-667-0921. TWX 910-930-9021.

Circle No. 358

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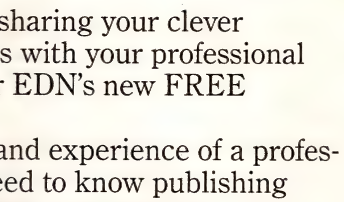

Get your FREE copy of EDN's writer's guide by circling number 800 on the Information Retrieval Service Card or by calling (617) 964-3030.

Industrial PC

- *Contains 20 16-bit passive ISA bus expansion slots*
- *Metal chassis contains 350W power supply*

The 5300 industrial computer has 20 16-bit passive ISA bus expansion slots. Its metal chassis contains a 350W power supply with 0.5% regulation and two cooling fans with air filters. The 18-in.-deep chassis can reside on a desktop or in a 19-in. rack, and it can accommodate as many as six disk drives. CPU boards are available with either an 80286 or an 80386 µP and as much as 16M bytes of RAM. Controller boards are available for either two half-height 3½- or 5¼-in. floppy-disk drives and four hard-disk drives. An IBM EGA- and VGA-compatible video controller card is also available. A system loaded with a CPU card provides 17 expansion slots for data-acquisition and communications boards. From $1850 for chassis, backplane, and power supply.

Systems Manufacturing Technology Inc, 1080 Linda Vista Dr, San Marcos, CA 92069. Phone (619) 744-3590. FAX 619-471-1153.

Circle No. 359

Its vast, electronic nervous system will transmit enormous amounts of information at the speed of light thanks to surface-mountable electronic components constructed of materials from Eastman Performance Plastics, such as the advanced Ektar® Filled Blend PCT Polymer.

Eastman is the only manufacturer of PCT, a material that allows the most efficient and economical manufacture of surface mounted components for vapor phase and infrared reflow-solderable printed circuit boards – the circuit boards of the future.

If miniaturization and surface mount technology are driving your need for better performance, greater reliability and increased economy, talk to us about Ektar® FB PCT Polymer and our full range of performing plastics. Call A. Laws at 1-800-EASTMAN or write to Eastman Performance Plastics, P.O. Box 1969, Kingsport, Tennessee 37664.

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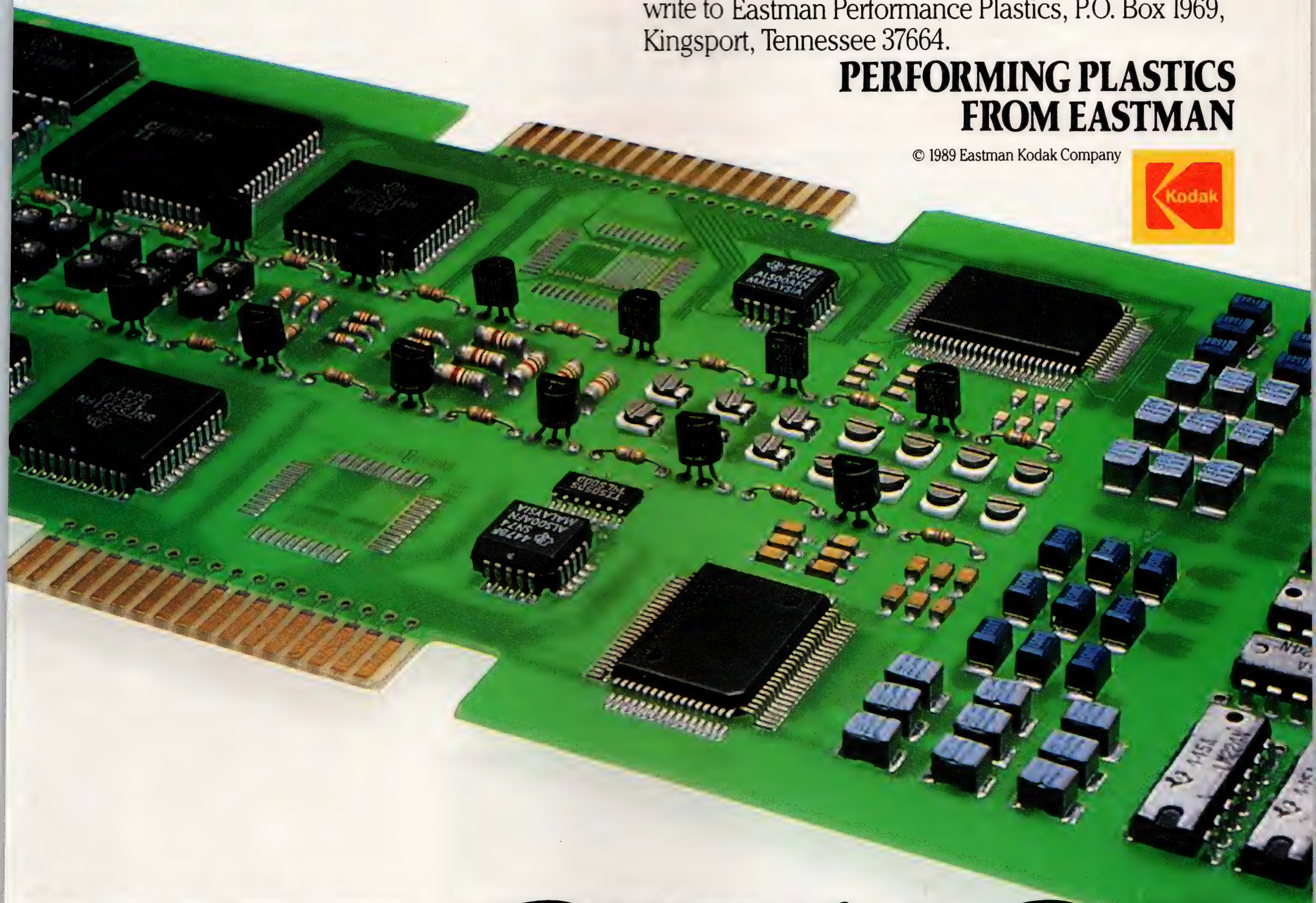


THE CITY OF THE FUTURE

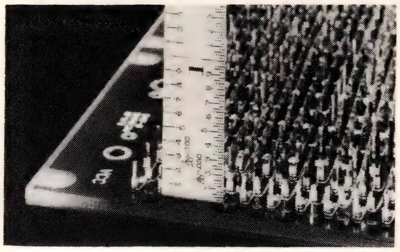
Ektar is a registered trademark of Eastman Kodak Company for its poly (1,4-cyclohexylene dimethylene terephthalate)

CIRCLE NO. 122

VMEbus Wire-Wrappable Boards

- *Pins for 4- to 5-turn wire-wrappable boards*
- *For VMEbuses with board pitches of 0.8 and 0.6 in.*

Two wire-wrappable boards are available for VMEbus systems that use either standard 0.8-in. or high-density board pitches. The boards have low-profile pins that accept two levels of a modified wire-wrappable board consisting of 4 to 5 turns each. This arrangement places the first wiring level directly on the reference plane and the second level closer to the reference plane that reduces the dielectric spacing between the plane and the wires. The boards are available in a variety of pin configurations and can accommodate as many as 252 ICs. The low-profile boards let you use 21 card slots in a 0.8-in. pitch VMEbus. An offset DIN connector lets you use 26 card slots in a 0.6-in. pitch system. $180 to $1800.



DataCon Inc, 60 Blanchard Rd, Burlington, MA 01803. Phone (617) 273-5800. FAX 617-273-4809.

Circle No. 360

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APPLICATIONS:
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(314) 423-4900 • TWX 910-764-0811 • FAX 314-423-3956

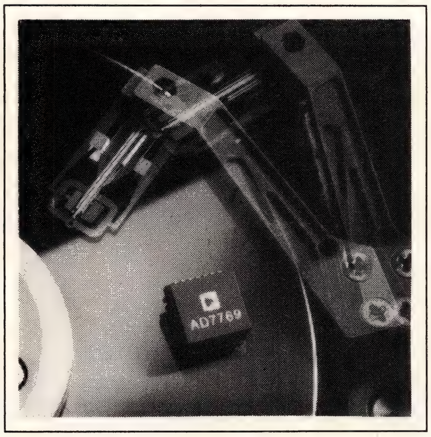
CIRCLE NO. 38

Communications Server

- *40 asynchronous devices connect to Ethernet*
- *Supports MIL-STD IP security communications*

The ACU2000 Version 3.45 communications server for Ethernet networks conforms to the IEEE-802.3 standard. The unit supports MIL-STD-IP security coding, which allows communications only between servers at the same security level. An 8-bit authority code permits as many as 256 different security-code combinations. The server can connect 40 asynchronous devices to TCP/IP (transmission control protocol/internet protocol) networks. You can join as many as four units to provide 160 network connections. Conditional macros let the user customize an interface to the particular needs of the site. The macros have the ability to branch, loop, and accept user inputs. An EEPROM stores as many as 15 macros of 255 bytes each. From $1050.

TRW Information Networks, 23800 Hawthorne Blvd, Torrance, CA 90505. Phone (213) 373-9161. FAX 213-375-5805. **Circle No. 361**



IC That Merges 8-Bit ADC, Two DACs On A Single Chip

- *Includes two buffer amplifiers*
- *Includes T/H amplifier*

Because of its high level of integration, the AD7769 can replace as many as eight separate devices. Used as an analog I/O port, the device combines a 2-channel 8-bit ADC, two 8-bit DACs, a 200-kHz track-and-hold (T/H) amplifier, and two buffer amplifiers on a single chip. The typical conversion time of the ADC is 2.5 μsec to ±0.5 LSB; each DAC is buffered by an on-chip amplifier to deliver a typical 2.5 μsec settling time to ±0.5 LSB. The IC incorporates a biasing capability that lets users set the midpoint scales for the DACs and ADC, the full-scale input swing for the ADC, and the full-scale output swing for the DACs. Other specifications include ±1-LSB max relative accuracy, ±1-LSB max differential nonlinearity, full-scale matching of the two DACs to ±4 LSB, a 44-dB signal-to-noise ratio, −48-dB THD, and −60-dB intermodulation distortion for the ADC and −55-dB for the two DACs. The AD7769 has a bus-access time of 65 nsec and a write-pulse width of <90 nsec. In a 28-pin DIP or a 28-pin PLCC (plastic leaded chip carrier), from $13 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TLX 924491. **Circle No. 368**

Zero-Power Programmable Logic Sequencer

- *Operates to 16 MHz*
- *Standby current is 100 μA*

According to the company, the PLC415-16 is the industry's first programmable logic sequencer (PLS) with zero-power capability. The device is guaranteed to operate to at least 16 MHz and features a

Vitelic's Memory Lineup for Big League Personal Workstations.

RICKY SIMM
256K x 8 and 256K x 9 DRAM modules in 70, 80, and 100ns speeds. Also available in SIP version.

GRAND SLAM VRAM
Dual Port architecture, 64K x 4 Video RAM with 80ns access time.

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Fast, low power 8K x 8 and 2K x 8 SRAMs available in DIP and surface mount packages.

SLUGGER DRAM
High performance 256K and 1 Meg DRAMs for 0 Wait State system performance. x4 and x8 DRAM configurations for high bandwidth PC graphics.

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8K x 16 Cache SRAM optimized for 20-33MHz Intel 386SX, 386, and 486 systems. Easily interfaces with Intel, Chips & Technologies, and Austek controllers.

THE INTERFACE BROTHERS
- 512K x 9 and 1K x 9 FIFOs with access times to 35ns.
- 2K x 8 Dual Port SRAM with on-chip arbitration and access times to 70ns.

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Circle 32 for Literature

Circle 33 for Demonstration

standby current of only 100 μA. Normal operating current is 80 mA max. The IC's programmable OR architecture, buried registers, and output registers make it suitable for synchronous Mealy functions, which are often used in sequencing and control applications. In addition to the power-down feature, the IC offers output-enable and asynchronous-initialization control. These user-programmable functions allow you to individually customize both preset and reset functions to any predetermined pattern. The 28-pin device has 17 inputs, eight buried registers for state-transition storage, eight output registers for clocked-output transactions, and 68 AND product terms. Support for the PLC415-16 is provided by the company's Amaze PLD design software, which runs under MS-DOS 2.1 and later revisions. $12 to $15 (1000), depending on packaging.

Signetics Co, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-5078. **Circle No. 369**

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Audio A/D Converter

- *Features 20-bit resolution*
- *Capable of 128× oversampling*

Based on an oversampling, noise-shaping architecture, the ADC-20048 converts audio-bandwidth signals at a 128× sampling rate. This oversampling of the nominal 44.1- or 48-kHz data rates used for audio signals eliminates the need for antialias filters and greatly reduces differential nonlinearity and harmonic distortion for low-amplitude signals. The ADC-20048 is a 2-chip set comprised of the AFE 20048 Analog Front End, which comes in a 2×3×0.4-in. epoxy-encapsulated module, and the D20C10 Decimator IC, which comes in a standard 48-pin DIP. Performance specifications over the 20-Hz to 20-kHz audio range include a S/N ratio of 110 dB, THD of −96 dB at an output of −2 dB and −50 dB at an output of −60 dB, and quantization error of ±0.5 LSB. The converter accepts full-scale input voltages of either ±3 or ±5V, and operates from ±15 and 5V supplies. $275 (single qty); $169 (250).

UltraAnalog Inc, 47747 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 657-2227. FAX 415-657-4225. **Circle No. 370**

4M-Bit EEPROM Hybrid

- *User configurable in three modes*
- *Operates from a single 5V supply*

The M4194E is an uncommitted 4M-bit EEPROM that is configurable in any of three modes: 512k×8 bits, 256k×16 bits, or 128k×32 bits. The

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ORGANIZATION	PACKAGES	SPEED
SRAM MODULES		
128K X 8	32-PIN DIP	30, 35, 45
64K X 16	40-PIN DIP	30, 35, 45
32K X 16	40-PIN DIP	30, 35, 45
64K X 32	64-PIN ZIP	25, 30, 35, 45
16K X 32	64-PIN ZIP	15, 20, 25, 30, 35, 45
DRAM MODULES*		
512K X 36	SIMM/ZIP	80, 100, 120
256K X 36	SIMM/ZIP	80, 100, 120
1MEG X 8/9	SIMM/SIP	80, 100, 120
256K X 8/9	SIMM/SIP	80, 100, 120, 150
64K X 8/9	SIMM/SIP	80, 100, 120, 150
64K X 4/5	SIMM/SIP	80, 100, 120, 150

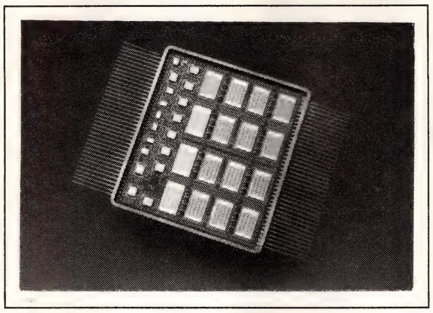
* Micron offers a variety of packages configured in both standard and low profile versions. Access Cycles offered are Fast Page Mode, Page Mode, Static Column and Nibble Mode.

MICRON
TECHNOLOGY, INC.

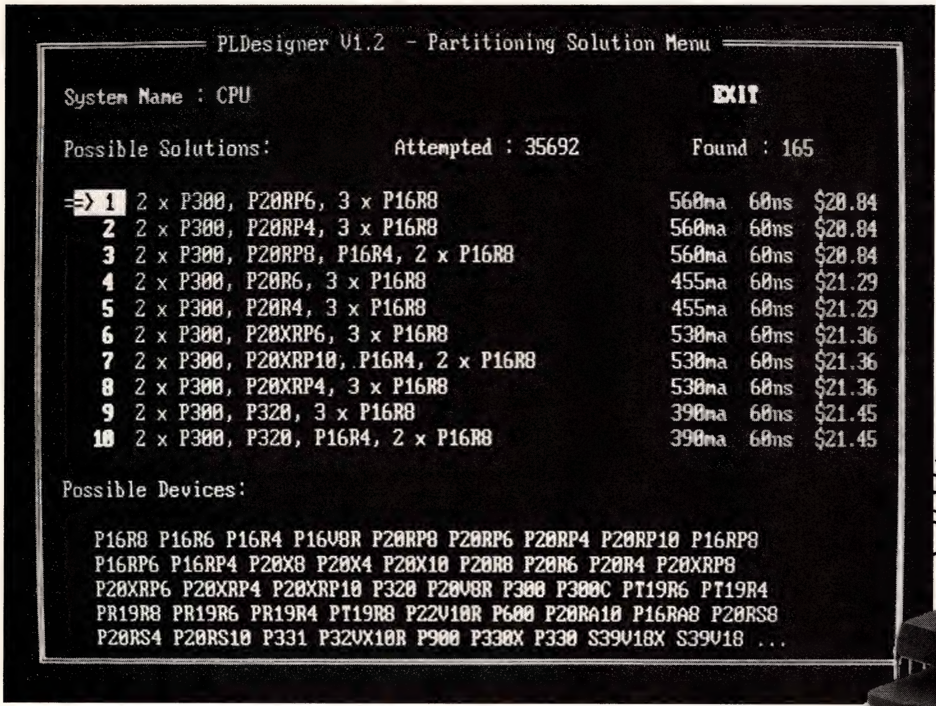
2805 E. Columbia Road, Boise, Idaho 83706 208-386-3900

CIRCLE NO. 123

user makes the choice when the hybrid module is soldered to the pc board; the grounded pin determines the bit mode. The EEPROM is usable with virtually any 8-, 16-, or 32-bit µP including the Z8000, 8086, 80286, 80386, MC68010, and MC68020. The M4194E also supports multiprocessor operation in that bytes written in the 8-bit mode can be read in the 16- or 32-bit mode with total word (double word) integrity. The hybrid module, which comes in a 1.9×2.1-in. hermetically sealed, 76-pin flatpack, contains 16 32k×8-bit memory cells plus 19 other ICs for buffers, latches, decoders, control logic, byte selection, and timing. Operating from a single 5V supply, the maximum operating current at 25°C is 83 mA for the 8-bit mode, 163 mA for the 16-bit mode, and 323 mA for the 32-bit mode. Standby current in all modes is 3 mA, and the maximum access time is 150 nsec. The device features 10-year data retention. $2400 (100).



White Technology, 4246 E Wood St, Phoenix, AZ 85040. Phone (602) 437-1520. **Circle No. 371**



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PLDesigner V1.2  - Partitioning Solution Menu

System Name : CPU                                       EXIT

Possible Solutions:          Attempted : 35692        Found : 165

=> 1  2 x P300, P20RP6, 3 x P16R8                  560ma  60ns  $20.84
   2  2 x P300, P20RP4, 3 x P16R8                  560ma  60ns  $20.84
   3  2 x P300, P20RP8, P16R4, 2 x P16R8           560ma  60ns  $20.84
   4  2 x P300, P20R6, 3 x P16R8                   455ma  60ns  $21.29
   5  2 x P300, P20R4, 3 x P16R8                   455ma  60ns  $21.29
   6  2 x P300, P20XRP6, 3 x P16R8                 530ma  60ns  $21.36
   7  2 x P300, P20XRP10, P16R4, 2 x P16R8         530ma  60ns  $21.36
   8  2 x P300, P20XRP4, 3 x P16R8                 530ma  60ns  $21.36
   9  2 x P300, P320, 3 x P16R8                    390ma  60ns  $21.45
  10  2 x P300, P320, P16R4, 2 x P16R8             390ma  60ns  $21.45

Possible Devices:

  P16R8 P16R6 P16R4 P16V8R P20RP8 P20RP6 P20RP4 P20RP10 P16RP8
  P16RP6 P16RP4 P20X8 P20X4 P20X10 P20R8 P20R6 P20R4 P20XRP8
  P20XRP6 P20XRP4 P20XRP10 P320 P20V8R P300 P300C PT19R6 PT19R4
  PR19R8 PR19R6 PR19R4 PT19R8 P22V10R P600 P20RA10 P16RA8 P20RS8
  P20RS4 P20RS10 P331 P32VX10R P900 P330X P330 S39V18X S39V18 ...
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PLDesigner uses your design philosophy when scanning its library of over 2500 different parts. Possible devices have architectures appropriate to implement the design. Attempted solutions are the combinations of possible devices. Of these combinations, 165 viable solutions were found. You can then choose from the top ten implementations displayed. Power consumption, propagation delay and estimated cost given for each solution ensure that the final implementation you select is the most rigorous solution for your design problem.

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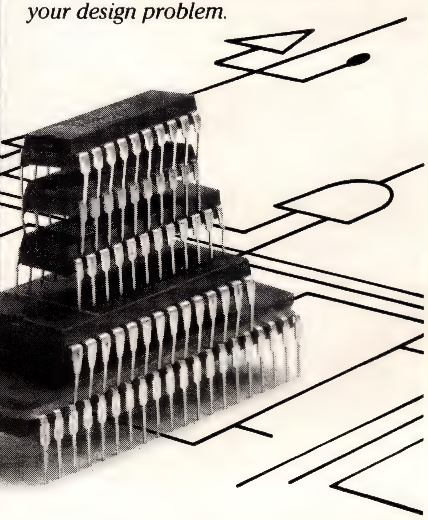

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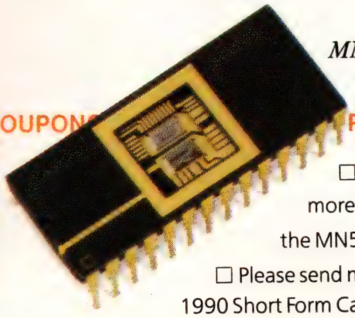

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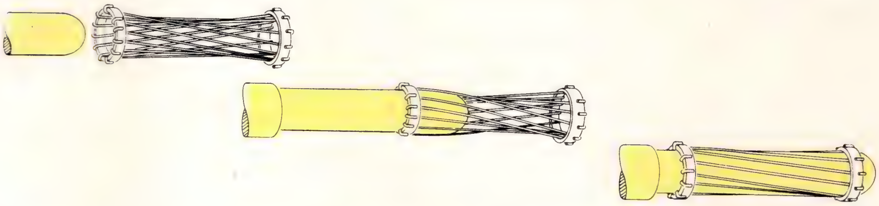

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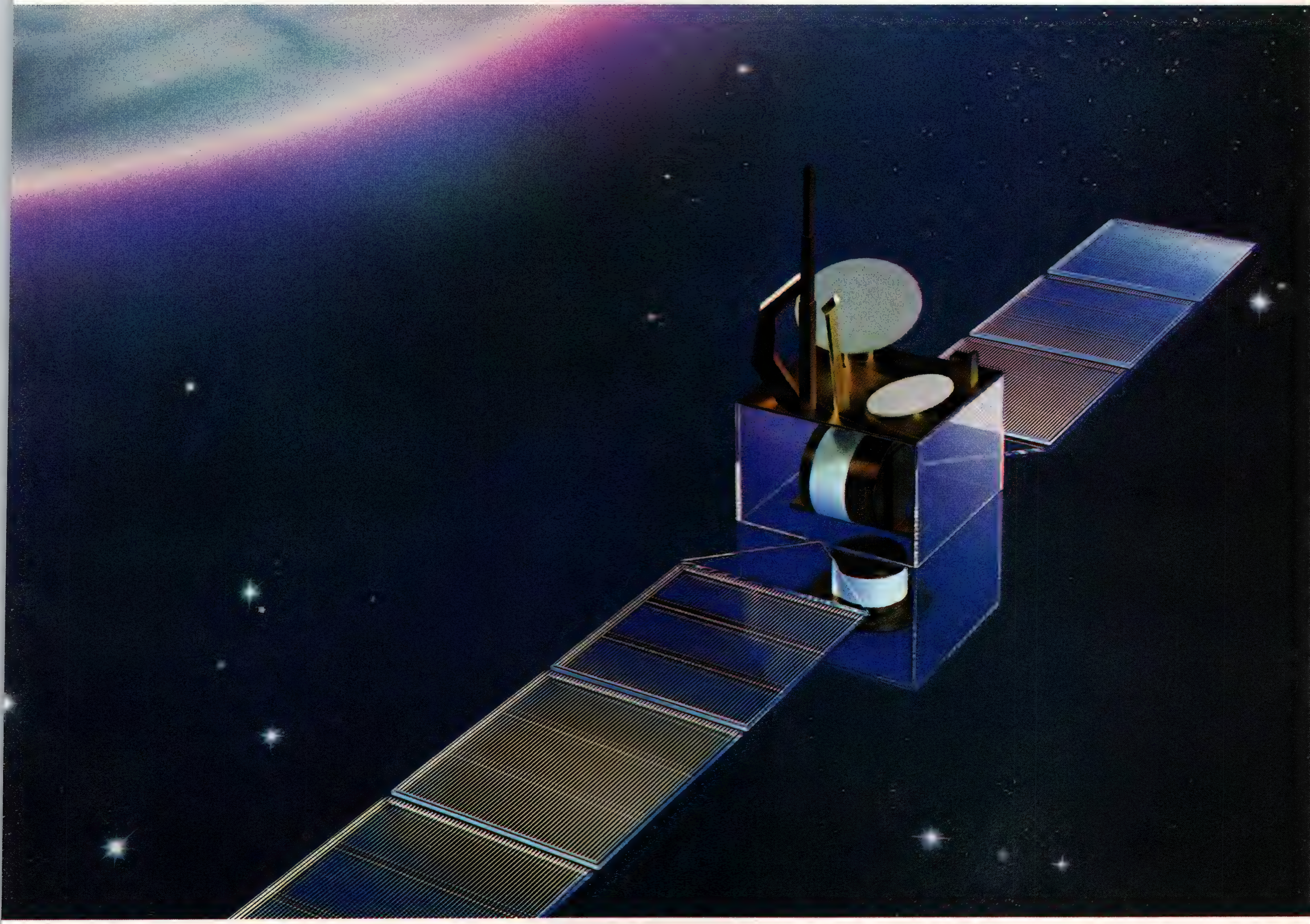

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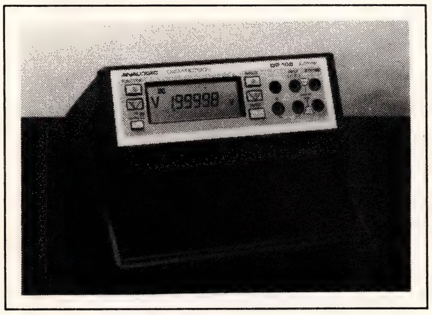
10-MHz Analog-Signal Isolators

- *Tolerate common-mode voltages to 1 kV*
- *Provide 80 dB of CMRR at 1 kHz*

You can use the SL-10H and SL-10HV isolating signal links with a scope to safely view analog signals referenced to potentials as high as 1 kV. You can observe signals as small as a few tens of millivolts or higher amplitude signals with frequency components to 10 MHz. The units work with instruments whose input impedance is 1 MΩ in parallel with 15 to 30 pF or 50Ω. In addition to ohmically isolating your instrument's ground system from the unit under test, the isolators minimize measurement errors by providing common-mode rejection of approximately 110 dB at 10 Hz, 80 dB at 1 kHz, and 30 dB at 1 MHz. SL-10H with 10× input probe, $885; SL-10HV, with 1×, 10×, and 100× probes, $995. Delivery, four to six weeks ARO.

Signal Acquisition Technologies Inc, Box 753, Minden, NV 89423. Phone (503) 591-9445. FAX 503-642-4977. **Circle No. 362**



5½-Digit DMM

- *Includes frequency counter and rechargeable battery*
- *Has 1-year dc accuracy of 0.03% of reading plus two digits*

The DP100 5½-digit multimeter is based on a proprietary A/D conversion technique that makes minimum use of high-precision components. As a result, the vendor offers the meter at a price a little over half that of equally accurate competitive units with fewer features. The price is the same as that of units with accuracy almost an order of magnitude lower than the DP100's basic dc spec of 0.03% of reading plus two digits for one year after calibration from 18 to 28°C. You can calibrate the unit without removing its covers. The 3½-lb meter contains a battery that will operate it for 10 hours and recharge it in 16 hours. The meter also contains a true rms-to-dc converter for ac measurements, an RS-232C port, and a 25-MHz frequency counter with accuracy of 0.005% of reading plus two counts. The counter can resolve 1 Hz on its 200-kHz range. $595.

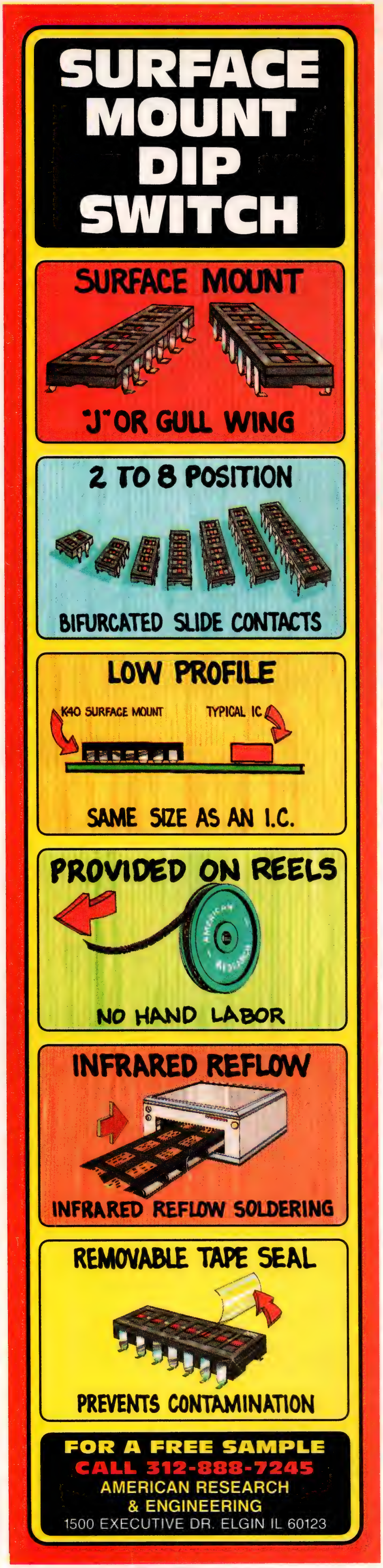
Analogic Corp, 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX 508-532-6097. TWX 710-348-0425.

Circle No. 363

68332 Emulation Tools

- *Hardware includes emulator and state/timing analyzer*
- *Software includes C compiler, assembler, debugger/simulator*

This set of development tools for Motorola's 68332 32-bit μC (microcontroller) is based on the tool vendor's HP 64700 in-circuit emulators and analyzers. The emulator, which works with Motorola's Business-Card Computer as well as the μC, plugs into a pin protector that matches the 68332's 132-pin plastic quad flatpack. To simplify symbol referencing, the emulator automatically translates chip-select lines; to facilitate interpreting trace displays, it dequeues trace data. The emulator also lets you display and modify registers in all of the 68332's on-chip peripherals. The tool set includes a C compiler optimized for the 68332, an assembler fully com-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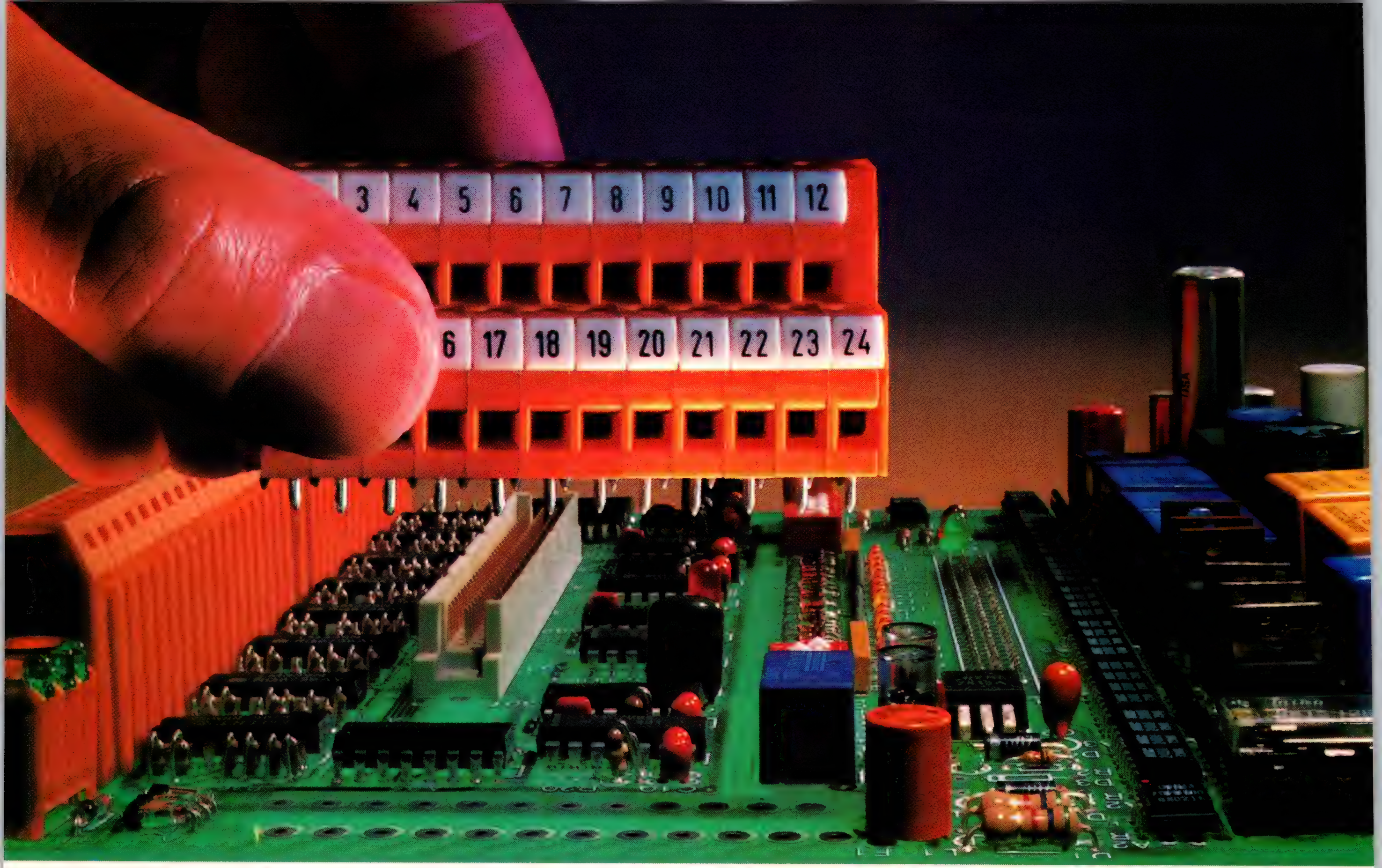

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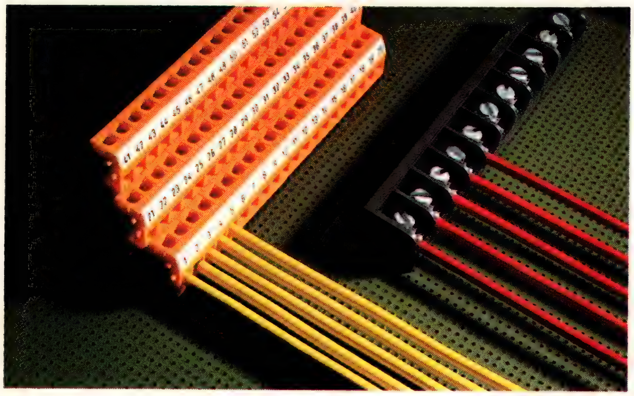

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Weidmuller's high-density terminal blocks deliver five connections per inch. And you can further increase the value of your real estate with our double- and triple-level blocks.

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For example, our BLA/SLA PC board connectors are made from 94 V-0 rated PBTP for tight dimensional tolerances even in harsh, high-heat, high-humidity environments. And our unique screw clamp system gives you a reliable vibration-proof connection. So when you're designing your next PC board, move to the block built for high density. Specify Weidmuller.

To receive Weidmuller's easy-to-use product guide, write for our free "Wire-To-Board Product Selection Chart," at 821 Southlake Boulevard, Richmond, Virginia 23236, 804/794-2877.

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Electrical and Electronic Connection Systems

Weidmuller terminal blocks are approved for use by UL, CSA and VDE.

CIRCLE NO. 129

patible with Motorola assembly language, a debugger/simulator for both C and assembly code, and a basis branch analyzer that identifies branches exercised during software testing. Emulation subsystem, $16,800; 16-channel state/timing analyzer, $2700; software tools, $7115.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 364

EEPROM Programmer

- *Has 32- and 40-pin sockets*
- *Without adapters, programs 24- to 40-pin devices*

With both 32- and 40-pin zero-insertion-force sockets, the EZ-Writer-K3 programmer for EPROMs and EEPROMs accommodates most such ICs in 24- to 40-pin DIPs without using adapters or personality modules. The unit's panel sports a 40-character LCD and only three keys. By using up- and down-arrow keys, you scroll through plain-English menus. Pressing the execute key invokes the displayed choice. The programmer's internal memory stores 256k bytes and expands to 2M bytes. You can also add external adapters for gang and set programming and for programming µCs. An RS-232C port lets you use the unit with external terminals and computers. $795..

Bytek Corp, 508 NW 77th St, Boca Raton, FL 33487. Phone (407) 994-3520. FAX 407-994-3615.

Circle No. 365

200-kHz FFT Analyzer

- *Analyzes analog signals in frequency domains*
- *Performs as spectrum, network, and waveform analyzer*

The 2642 personal Fourier analyzer is an IBM PC-based instrument that simultaneously characterizes analog waveforms in the dc- to 200-kHz band in the time and frequency

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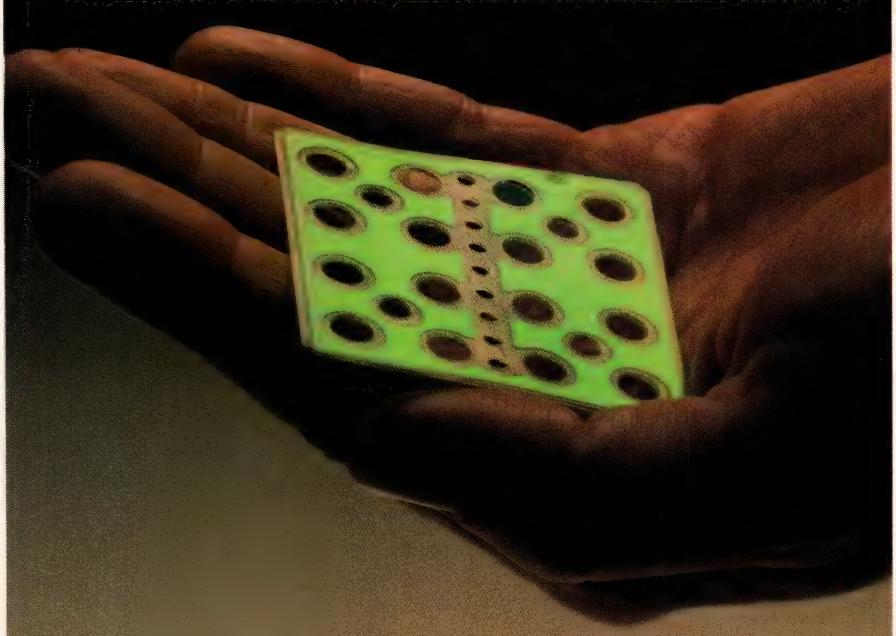

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Our DC-AC inverter line is performance-matched to provide the optimum power source for specific lamp size, geometry and output.

SEND FOR OUR DESIGN GUIDE. IT'LL SHED MORE LIGHT.

When it comes to electroluminescence, we've quite literally written the book. And we'd like to send it to you – the DESIGN GUIDE. Because when you spend a lot of time making your product and your reputation solid, lighting shouldn't be its weakest link.

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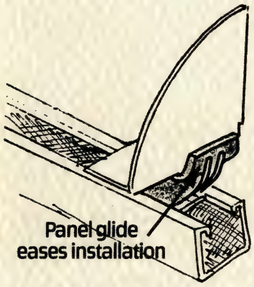

Your imagination needn't ever again be limited by an enclosure. Introducing the new Hoffman Designline™2 D-20 electronic enclosure with both rack and panel mounting.

The new panel mounting capability is just the first of many ways we've improved the D-20.

An economical double-wide version is now available. Multiple D-20s can be securely joined to form a single unit. Access can be made from all sides. And we've even incorporated a new disconnect capability.

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To help you discover how the D-20 can give you increased flexibility and protection, we've created a free brochure. To receive it, circle the number below or write us at 900 Ehlen Drive, Anoka MN 55303. Or call (612) 421-2240. Ask about our free Selection Software Disc, too.

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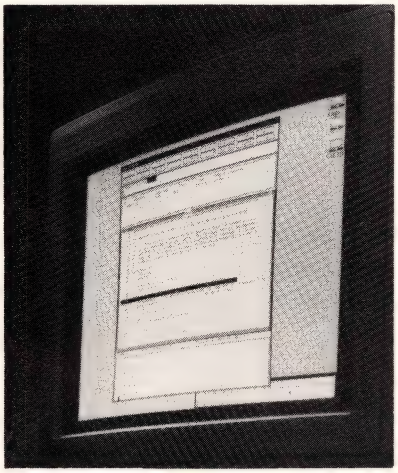
CIRCLE NO. 130

domains. According to the vendor, the 2642 is the first unit in its class to operate beyond 100 kHz. Besides functioning as a spectrum and a network analyzer—for example, by measuring frequency response and power spectra and accumulating time records—the unit performs operations such as auto- and cross-correlation, and ⅓-octave analysis in real time. By postprocessing, the unit can analyze data in other ways. The operator interface uses color graphics, a mouse, and pull-down menus. $19,500. Delivery, six weeks ARO.

Tektronix Inc, Box 19638, Portland, OR 97219. Phone (800) 234-1256. **Circle No. 366**



Real-Time Software Development/Debug Tools

- *Provide source-level C cross-compiler and -assembler*
- *Facilitate 680x0 code development on Sun workstations*

The Validate/Unison software-development package includes a C source-level cross-debugger based on Intermetrics' XDB, an optimizing cross-compiler, a cross-assembler, and associated utilities. The package, which runs on IBM PC-compatible computers, VAXs, and Sun and Apollo workstations operating under MS-DOS, Unix, VMS, Ultrix, and Aegis, works with the vendor's ES 1800 series of in-circuit emulators. The Validate/Unison supports seven processors in the 80x86 family and four in the 680x0 family. The latest release of Validate/XEL, which works with the ES 3200 series as well as the ES 1800, simplifies development of code for the 680x0 family on Sun workstations. Versions are also available for IBM PC-compatible computers and DEC VAXs. Validate/Unison, from $3300; Validate/XEL, from $5000.

Applied Microsystems Inc, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; in WA, (206) 882-2000. FAX 206-883-3049.

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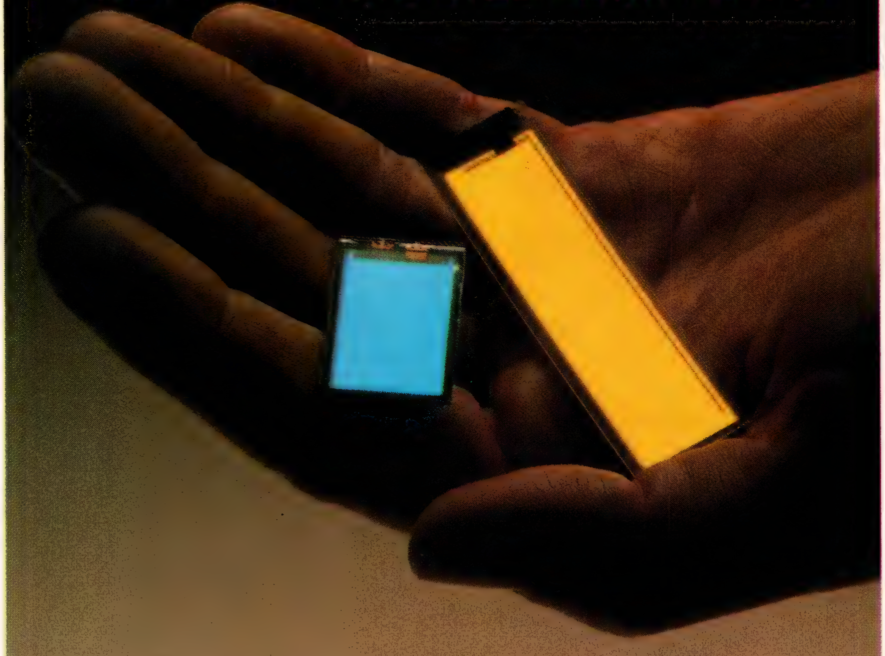

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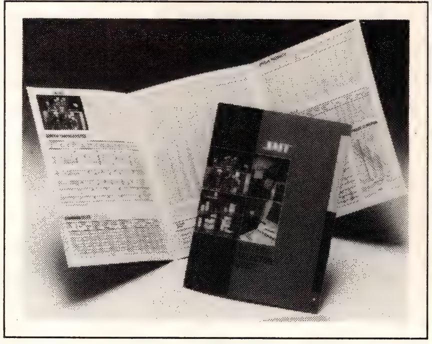
CIRCLE NO. 44

Guide aids battery selection

The vendor's 6-pg fold-out guide features a chart to help you choose the NiCd or lithium batteries you need. The selection includes standard cells, high-temperature Polytemp cells, and fast-charge, low-resistance cells. Other batteries listed include the VE series for rapid-charge, high-energy applications and the ultra-thin GP series that provides as much as 70% more volumetric energy for use in small personal appliances. The publication lists specifications, including rated capacity; the rates for charge, temperature, and discharge; and the size of each cell. The brochure also explains both solid- and liquid-cathode lithium batteries.



Saft America Inc, 711 Industrial Blvd, Valdosta, GA 31601.

Circle No. 372

Publication presents data-acquisition system

This 12-pg brochure details the proprietary data-acquisition system, AutoNet. Included in the package are general and technical information and separate specification sheets on the variety of hardware and software modules you can use to customize your applications.

Imagination Systems, 5752 Princess Anne Rd, Virginia Beach, VA 23462. **Circle No. 373**

Brochure features data-acquisition products

This 12-pg booklet contains the vendor's complete line of data-acquisition equipment, including PC-based data-acquisition software and front ends; stand-alone data loggers; multipoint hybrid recorders; and other data-acquisition products. Highlighted in the publication is the 2286A data logger, which can expand to 1500 channels and has a built-in, MS-DOS-compatible μfloppy-disk drive. Also featured is the Helios Plus data-acquisition front end, which has high measurement accuracy and a fast ADC.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206.

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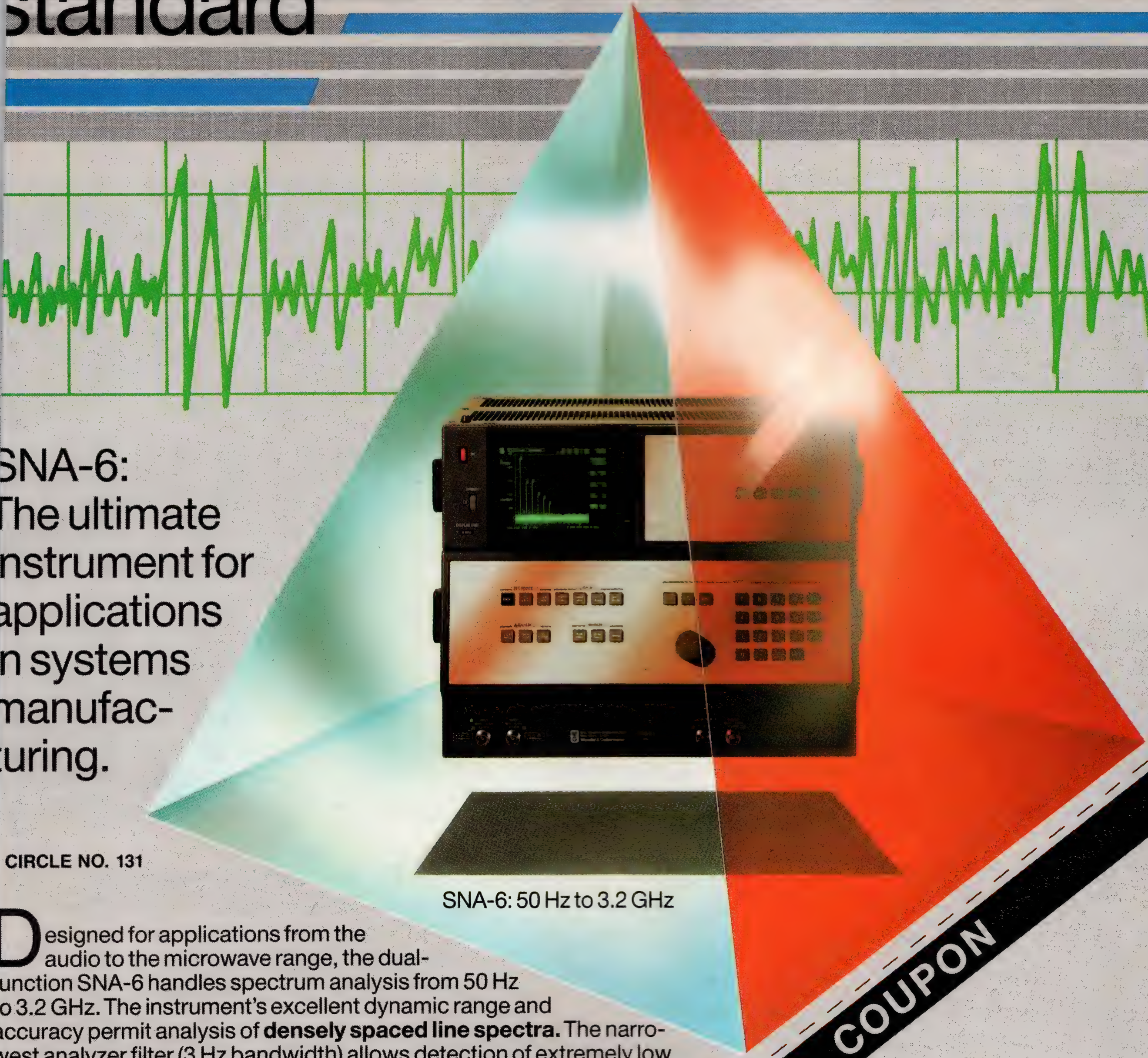
The new performance standard



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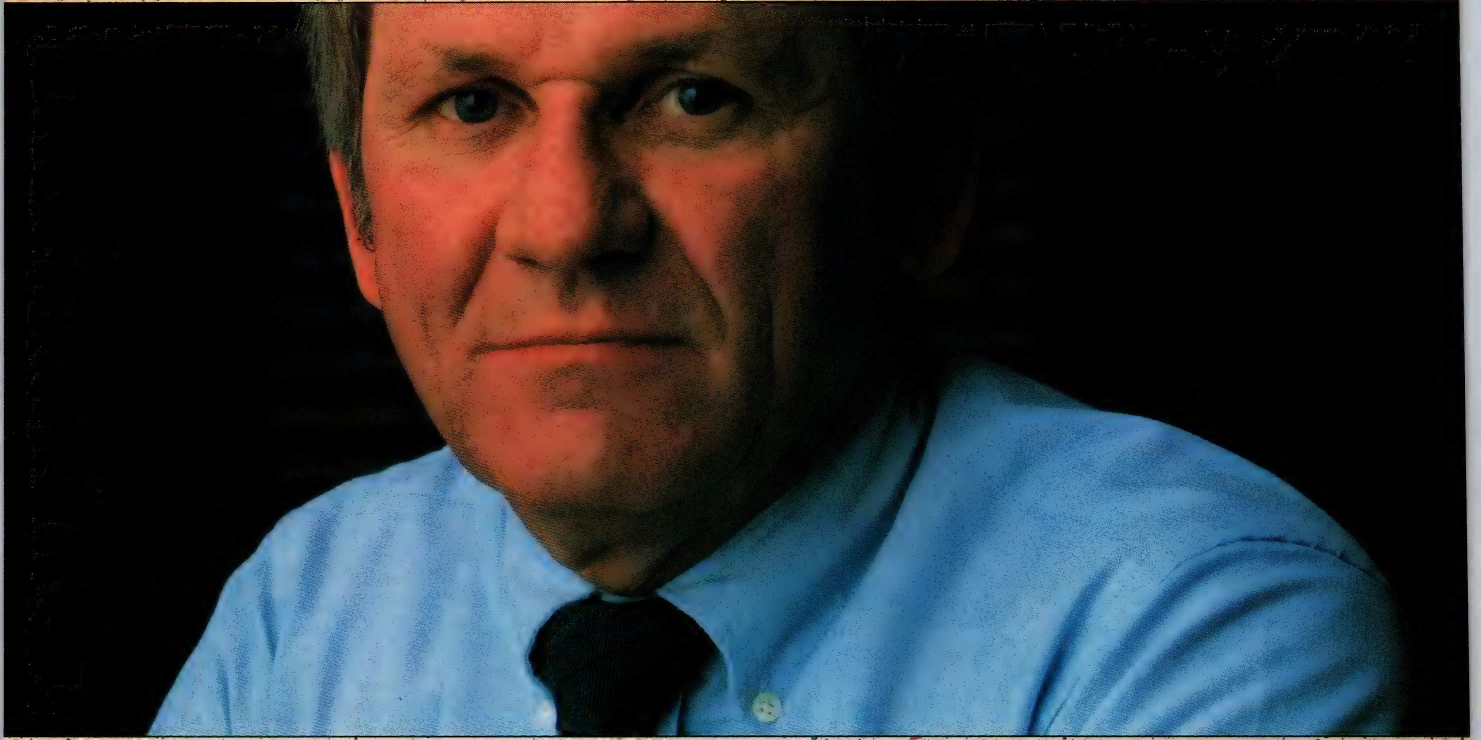
“An interconnect supplier who can’t act like a partner is off my list.”



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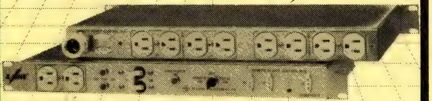

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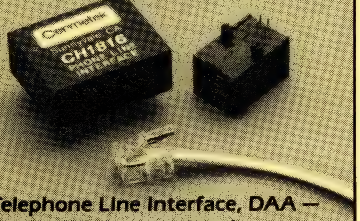

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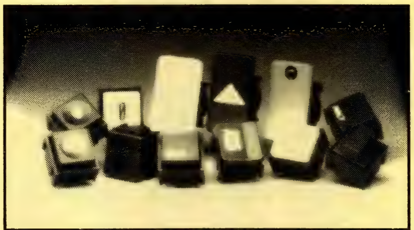

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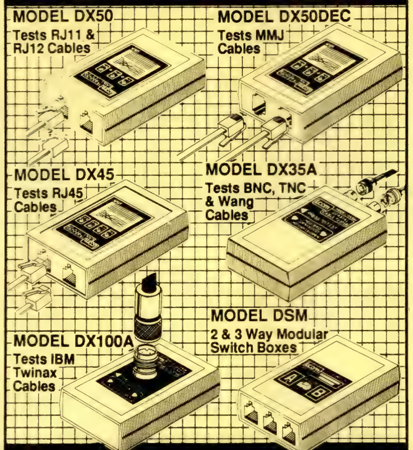

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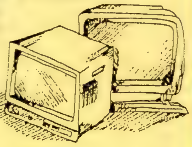

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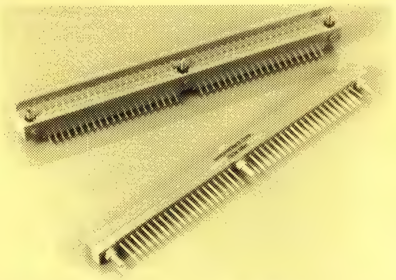

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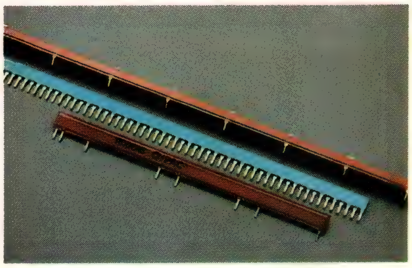

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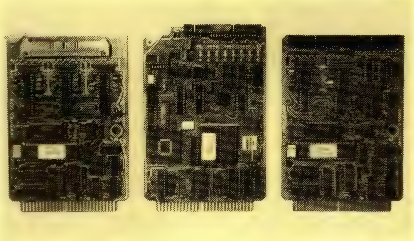

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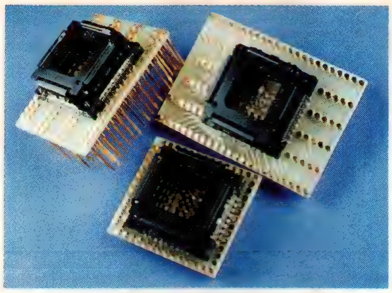

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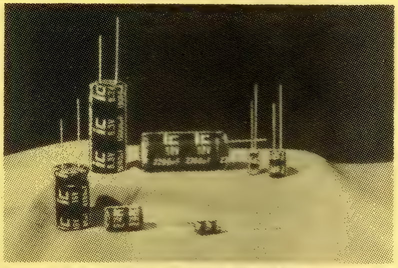

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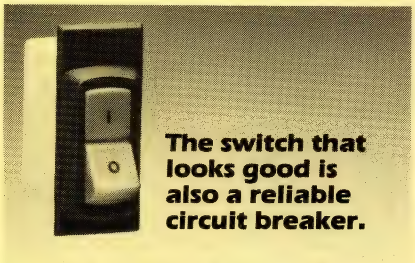
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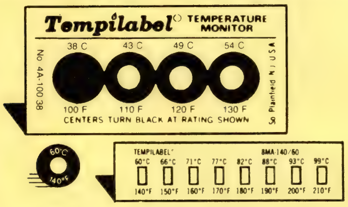
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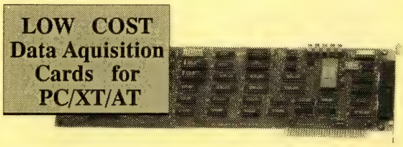

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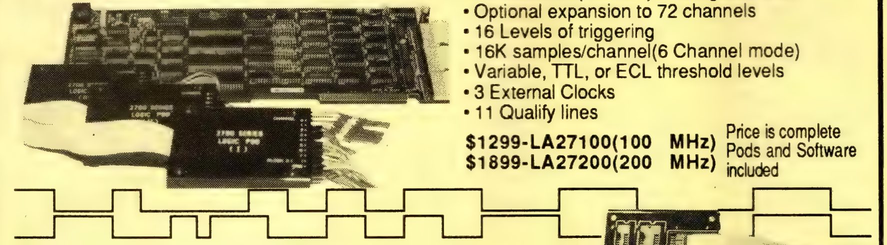

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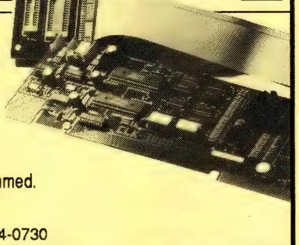

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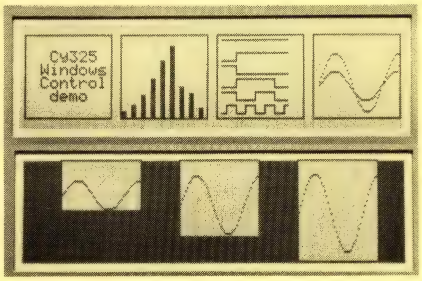

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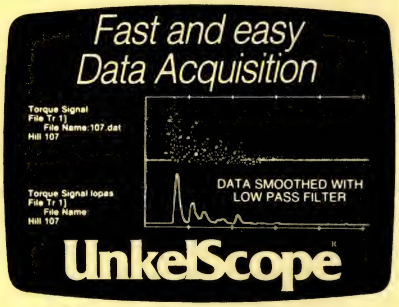

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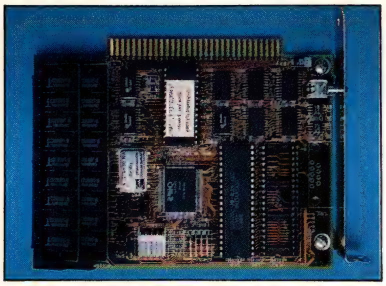

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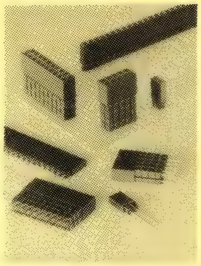

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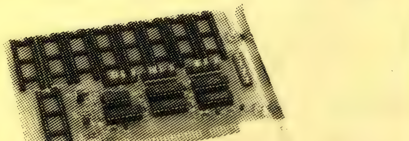

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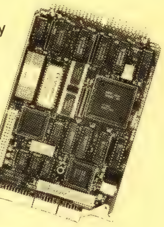

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```
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typedef struct {
   int foo;
   double bar;
   char baz[36];
} quux;

/***    foobar  inspect baz in a quux
*/

static quux * foobar(                quuxptr)
   int bar;
   quux * quuxptr;
{
   int i;

   for (i = bar
      if (quuxptr
         return (quuxptr);

   return (NULL
}
-- More --
```

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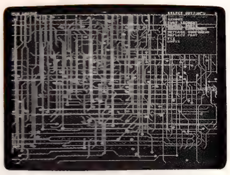

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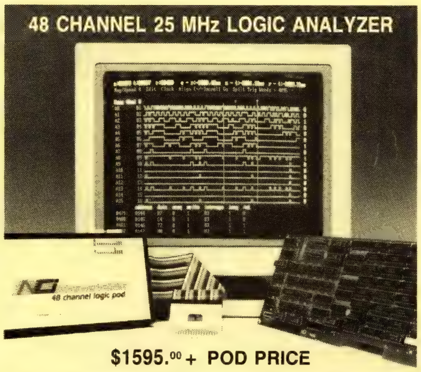

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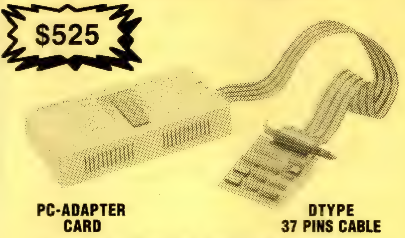

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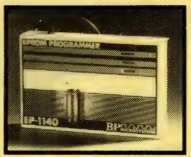

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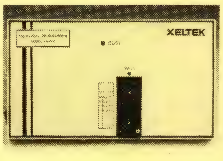

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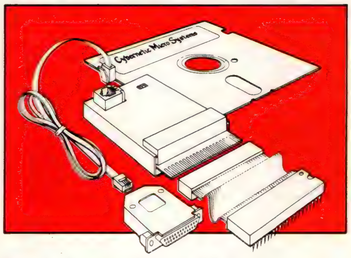

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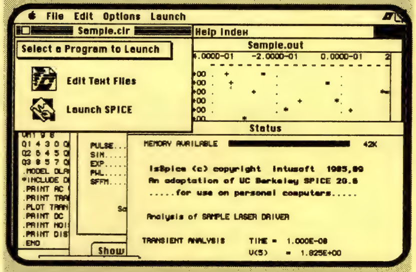

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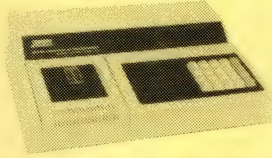

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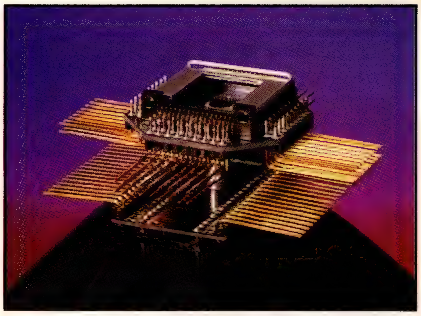

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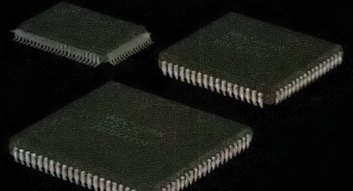

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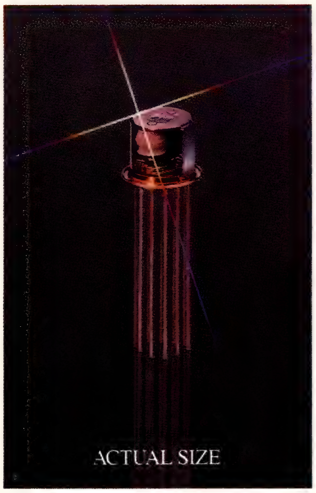
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CIRCLE NO. 134

Owen Garriott

Engineer, astronaut, scientist, educator—some people do it all.

Jay Fraser, *Associate Editor*

Photograph by Fred Myers

Until he was 35 years old, Owen Garriott believed teaching was going to be his lifelong career. He had earned his BSEE at the University of Oklahoma, served a hitch in the Navy, and then gone on to Stanford University, where he received his MS and PhD in electrical engineering. He had also been awarded a National Science Foundation Fellowship to study for one year at Cambridge University in England and at the Radio Research Station in Slough, near London.

After he completed his studies abroad, Garriott returned to Stanford and joined the faculty. He taught electronics, electromagnetic theory, and ionospheric physics. In just five years he became an associate professor. Then something happened that profoundly changed his life.

In 1965, NASA announced that it was looking for scientists who wanted to become astronauts. Garriott applied and was among the first six selected. After rigorous training, including 53 months of flight instruction, he was chosen for the second Skylab mission.

The mission ran into trouble almost as soon as it was launched. Less than one hour after lift off from Cape Canaveral on July 28, 1973, the spacecraft's pilot, Marine Major Jack Lousma, became motion sick. Soon the other two members of the crew—the commander, Navy Captain Alan Bean, and Garriott, the science pilot—were also feeling nauseated. Despite medication, all three were so sick the next morning they couldn't eat breakfast.

Although the astronauts managed to dock their command module with the orbiting Skylab, which NASA had launched two months earlier, they remained ill. On the second day of the mission, the module developed electrical problems. Shortly after that the primary cooling system sprang a leak. The men were able to make the necessary repairs, but they fell behind in their work schedule. Then their real problems began.

The pilot steered the spacecraft with four sets of four thrusters, called quads, located 90° apart on the hull. The quads were vital, not just to maneuver the module, but also to position it correctly for its reentry into the earth's atmosphere. Hitting the atmosphere at the wrong angle would cause the spacecraft to tumble and burn.

On the first day of the flight, one of the quads started to leak propellant and had to be shut off. Losing one quad was troublesome but not critical. The pilot could

***After returning to earth** following their 59-day Skylab mission, Jack Lousma (left) Owen Garriott (center), and Alan Bean (right) rest on the deck of the aircraft carrier* USS New Orleans.

still maneuver the module adequately with only three. Then on the sixth day in orbit, a second quad stopped functioning.

Mission Control became worried that there was some flaw in the design of the quads and that the other two would soon break down as well. If that happened, the astronauts would be stranded and helpless.

While NASA engineers frantically tried to determine what had gone wrong, flight controllers discussed whether or not to terminate the mission at once. They delayed a final decision because another spacecraft and crew were available in case a rescue became necessary.

By the next day, the engineers were satisfied that the malfunctions in the two quads were not related and there was no reason to assume the others would fail too. The flight controllers decided to let the flight proceed, although Lousma, Bean, and Garriott were now far behind schedule. NASA officials didn't have much confidence that the three astronauts could complete all the work that had been planned for them.

By the end of the mission, the crew had exceeded all of their original goals. NASA officials called the flight highly successful and noted that the astronauts had exceeded their objectives by 150%. NASA had wanted them to conduct 26 earth-resource surveys. They conducted 39. NASA had wanted them to spend 206 hours observing and photographing the sun. They spent 305. They took more than 100,000 photos of the sun, earth, and stars and recorded scientific data that filled 18 miles of audio tape. They returned with so much material that scientists needed years to analyze it all.

Garriott was busy throughout the mission. He made most of the scientific observations and took most of the photographs. He also spent six hours and 31 minutes outside Skylab in extravehicular activity—the longest "space walk" up to that time.

In his free time, Garriott performed and filmed a number of science demonstrations. They included experiments with gyroscopes, fluids, and magnetic effects in zero gravity. The demonstrations became the basis of a series of five science films, which millions of high school and college students have seen. Garriott planned the original experiments, filmed additional scenes in a laboratory on earth, and helped write the scripts. The mission offered him a perfect opportunity to combine scientific achievement and his skill as a teacher.

Although the mission had some serious problems, Garriott was never ill-at-ease or anxious while on board Skylab. "That could have some qualifiers added, like 'unduly' or 'inappropriately' anxious," he says with characteristic good humor. "But I always had confidence we had enough backup systems to get us back home if the need arose."

Counterbalancing the tense moments during the flight were a number of funny incidents. Some came about spontaneously. Others were carefully planned.

A mysterious voice from space

One day, instead of the expected routine radio transmission from the astronauts, the Capsule Communicator at Mission Control, Bob Crippen, heard a woman's voice say, "Hello, Houston. This is Skylab. Are you reading me down there?"

Crippen didn't say anything.

"Hello, Houston," the woman's voice repeated. "Are you reading Skylab?"

"Skylab, this is Houston," Crippen finally replied. "I heard you all right, but I had a little trouble recognizing your voice. Who have we got on the line here?"

"Roger, Houston. I haven't talked with you for a while. Is that you down there, Bob? This is Helen here in Skylab. The boys hadn't had a home-cooked meal in so long, I thought I'd just bring one up. Over."

The staff at Mission Control was listening to this conversation, dumbfounded. Crippen asked, "Helen, is that really you? Where are you?"

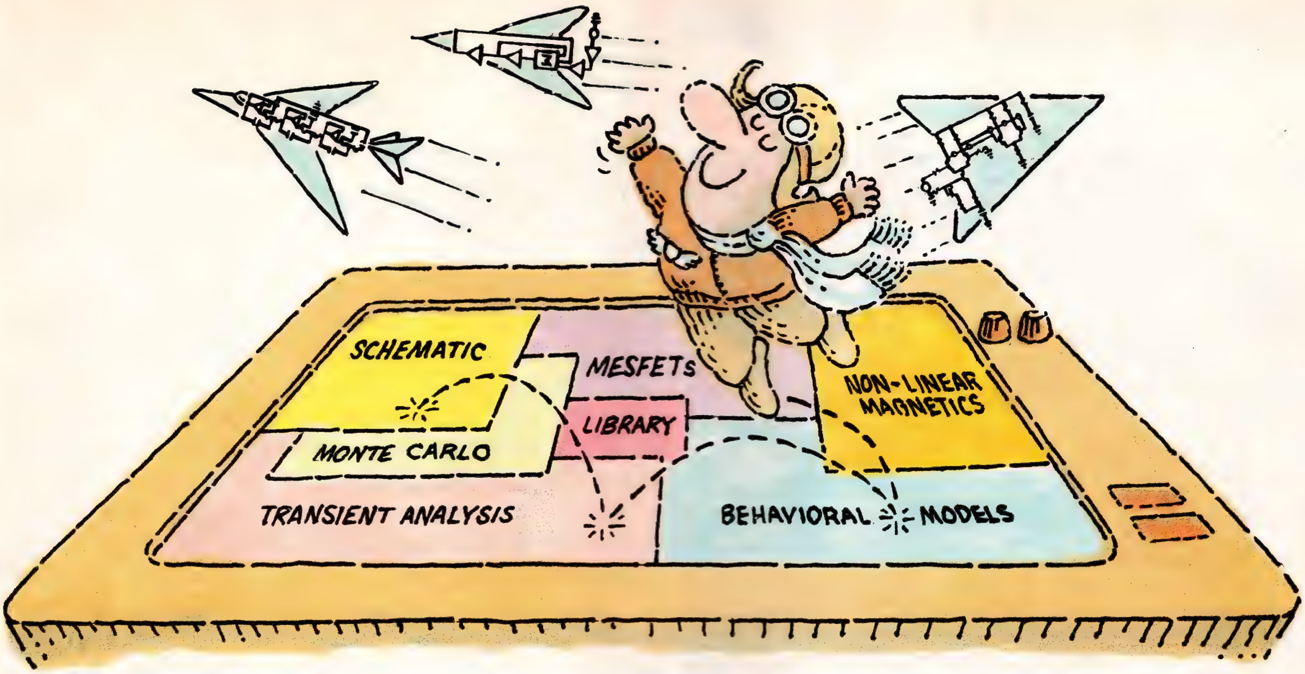
"Just a few orbits ago we were looking down on the forest fires in California. You know, the smoke sure does cover a lot of territory. And, oh, Bob, the sunrises are just beautiful.

"Uh-oh, I have to cut off now," Helen said quickly. "I see the boys are floating up toward the command module, and I'm not supposed to be talking to you. See you later, Bob."

"Bye, bye," said Crippen.

While the people at Mission Control stared at each other, speechless, the three astronauts burst out laugh-

Photography courtesy of NASA



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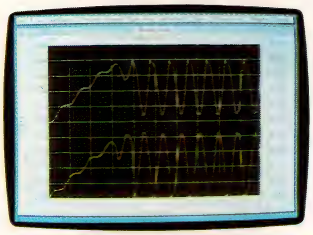
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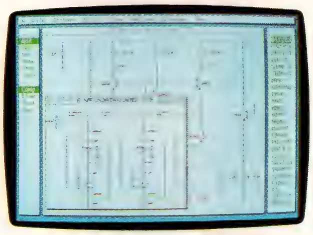
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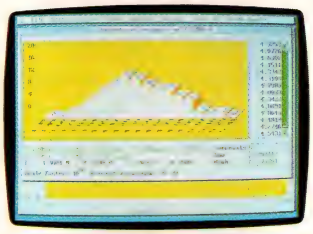
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Owen Garriott operates his ham radio *on board Spacelab. During the 10-day flight he contacted more than 300 hams on earth.*

Photography courtesy of NASA

ing. Garriott had taped his wife's voice before the mission, supplied Crippen and another capsule communicator with a script so their replies would be the correct length, and waited until he spotted either a hurricane or some forest fires on earth before playing the tape.

Even NASA's Public Affairs Office was fooled. "They said we must have recorded that at our private conversations, which we had with our families the night before we left," says Garriott. "In fact, it had been planned for over two months with two different capsule communicators and two different natural occurrences as a possibility."

Lousma, Bean, and Garriott splashed down in the Pacific Ocean on September 25, 1973. They had set a new record for time in space—59 days, 11 hours—and for distance covered—more than 24 million miles. They had done all the work and performed all the experiments that had been planned, and had often requested NASA scientists to devise new ones for them. Despite a poor start, the mission had been a resounding success.

After the Skylab flight, Garriott stayed with NASA. He became Deputy Director of Science and Applications at the Johnson Space Center in Houston, TX, then Director of Space and Life Sciences. In this second post, he was responsible for all physical-science research at the Center. He didn't retire as an astronaut, however, and remained available for future flights.

During this time, the 10-nation European Space Agency was developing Spacelab, a 6-man laboratory designed to be carried into orbit and returned to earth by a US space shuttle. Forty-nine companies in Europe and the United States had a hand in building it, and dozens of others supplied its instruments. It was larger, roomier, and more scientifically sophisticated than Skylab.

The first Spacelab crew consisted of a commander, a pilot, two payload specialists, and two mission specialists. Five of the astronauts were Americans, and one was a German. Owen Garriott, at age 53, was one of the mission specialists.

On November 28, 1983, the Space Shuttle Columbia lifted off from Cape Canaveral with Spacelab. The flight had little of the drama of the Skylab mission 10 years earlier. There were no major problems and only a few minor ones.

Columbia and Spacelab stayed in orbit for 10 days and circled the earth 166 times. The crew was divided into two 3-man teams, and each team worked a 12-hour shift. Besides making sure the laboratory itself performed properly, the crew carried out dozens of experiments in atmospheric physics, astronomy, life sciences, space plasma physics, materials processing, and fluid physics.

Garriott's duties on Spacelab were similar to those he had on Skylab. Once again he was busy observing and photographing the sun and stars and conducting earth-resource surveys.

"The principal difference between the two flights is that one lasted 10 days and the other lasted almost 60," says Garriott. "That long duration is much more compatible with the conduct of experimental work than the hurried-up arrangement of only 10 days and 50 or 60 experiments to do."

Among the personal possessions Garriott brought along was a ham radio. A lifelong amateur radio enthusiast, he had earned his call letters—W5LFL—when he was 15 years old. He assembled his 2-meter set inside Spacelab and placed its dipole antenna against one of the craft's windows. During his 10 days in orbit, he contacted more than 300 hams all over the world, including JY1—King Hussein of Jordan.

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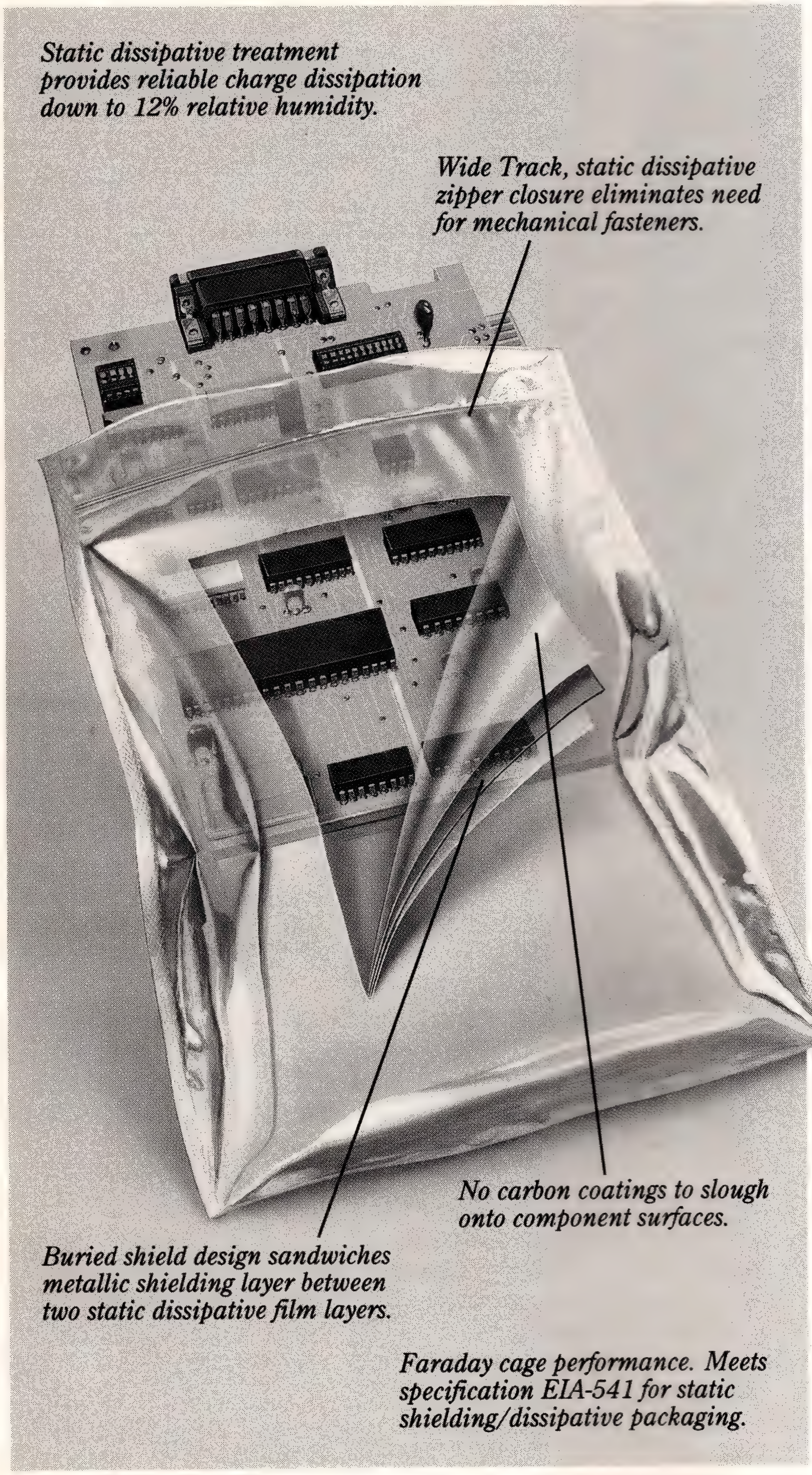

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***The Spacelab astronauts**, including Owen Garriott (bottom row, center), float freely in zero gravity.*

A controversy arose one week into the mission. President Ronald Reagan, West German Chancellor Helmut Kohl, and the Spacelab crew were scheduled to have a 3-way conversation on live television on December 5th. The White House didn't want to take any chances. Speechwriters prepared a script, and it was transmitted to Skylab for the men to follow. They resented this imposition. Then it was decided that only three of the astronauts would take part in the conversation. The others wouldn't even appear on camera. Garriott was one of those who would be left out.

The Spacelab crew complained about these conditions, but the White House wouldn't listen. The show would go on as planned. However, when the television technicians on earth turned on their monitors to run a test before the actual broadcast, they saw Garriott and the other two excluded astronauts facing the camera, each one holding his hands over his ears, eyes, or mouth in the classic "hear no evil, see no evil, speak no evil" pose.

NASA accepted this good-natured protest without comment, and the broadcast was done as planned. Three days later, Columbia and Spacelab landed smoothly and on schedule at Edwards Air Force Base in California. The 10-day flight was far shorter than the 2-month Skylab mission 10 years earlier, but it was a record for a space-shuttle trip up to that time. Spacelab had functioned well, and the crew had completed all its experiments. NASA considered the mission a complete success.

Photography courtesy of NASA

After the Spacelab flight, Garriott continued to work for NASA, this time as a program scientist in the Space Station Program Office at the Johnson Space Center. He was also preparing for another space flight. NASA was planning a special Environmental Observation Mission, and he was to be one of the crew. It never took place, however, because of the Challenger disaster.

After the Space Shuttle Challenger exploded, all shuttles were grounded indefinitely. "It was going to be too long before there was another flight," Garriott explains. "No one knew how long it was going to be. It turned out to be almost three years before the shuttle was flying again, and the mission I was assigned to still hasn't flown. I just didn't have that many years to wait for the next flight opportunity, so I thought I'd better do something different."

Garriott retired from NASA in 1986 and became president of a private firm involved in the development of a long-duration orbiter. In 1988, he joined Teledyne Brown Engineering in Huntsville, AL, as vice president of its Space Programs Division. He directs more than 800 people involved in a variety of projects for NASA, including the development of components for America's first space station, which is due to be assembled in orbit starting in 1993.

In addition, Garriott is still involved in education. He's a consulting professor at Stanford, and he recently gave a series of lectures about his space experiences at the University of Alabama at Huntsville. He thinks engineering schools today are doing a good job, but he sees some problems with education on the secondary and primary levels.

"For some reason, we're just not training our young people well in quantitative thinking," Garriott says. "I think that's a major flaw in our educational system.

"Teaching was my first profession, and I still have an affinity for it," he adds. "I probably would still be teaching at Stanford if it hadn't been for that unique opportunity that was provided by NASA." **EDN**

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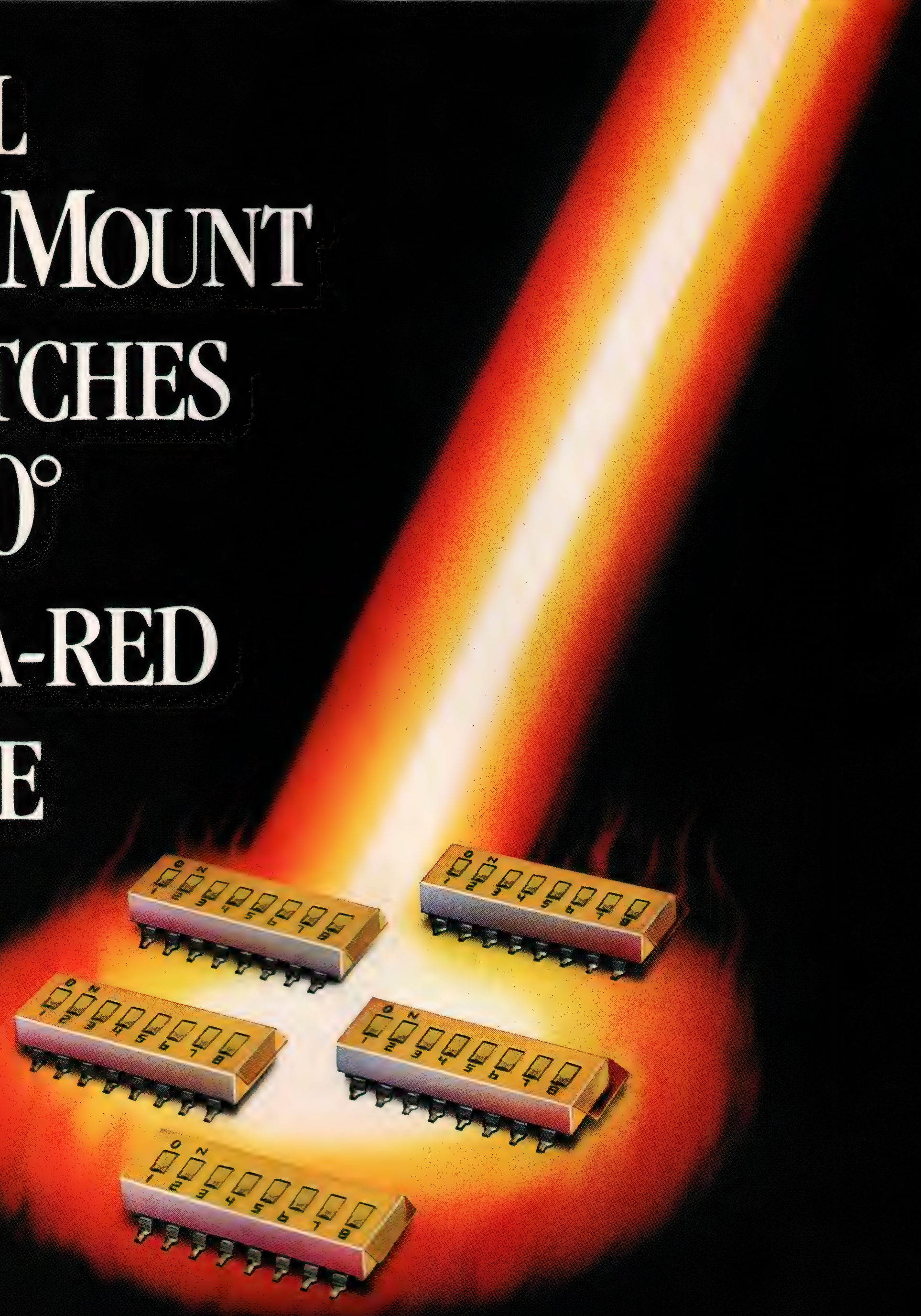

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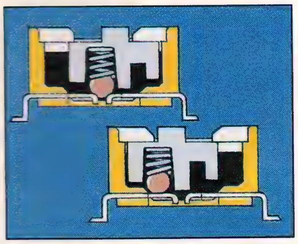

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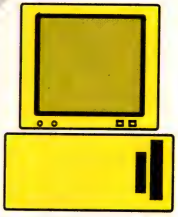

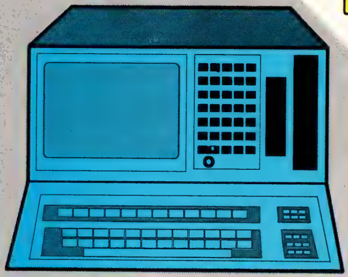

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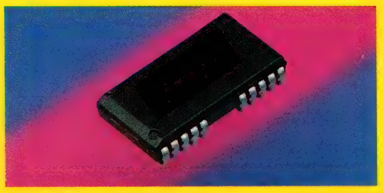

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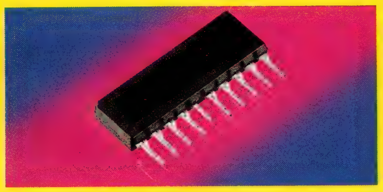

Any guesses who's now pulling off this staggering mega-double? And whom you should call a.s.a.p. for the latest information on the new 4 MBit DRAM? Turn over and find out.

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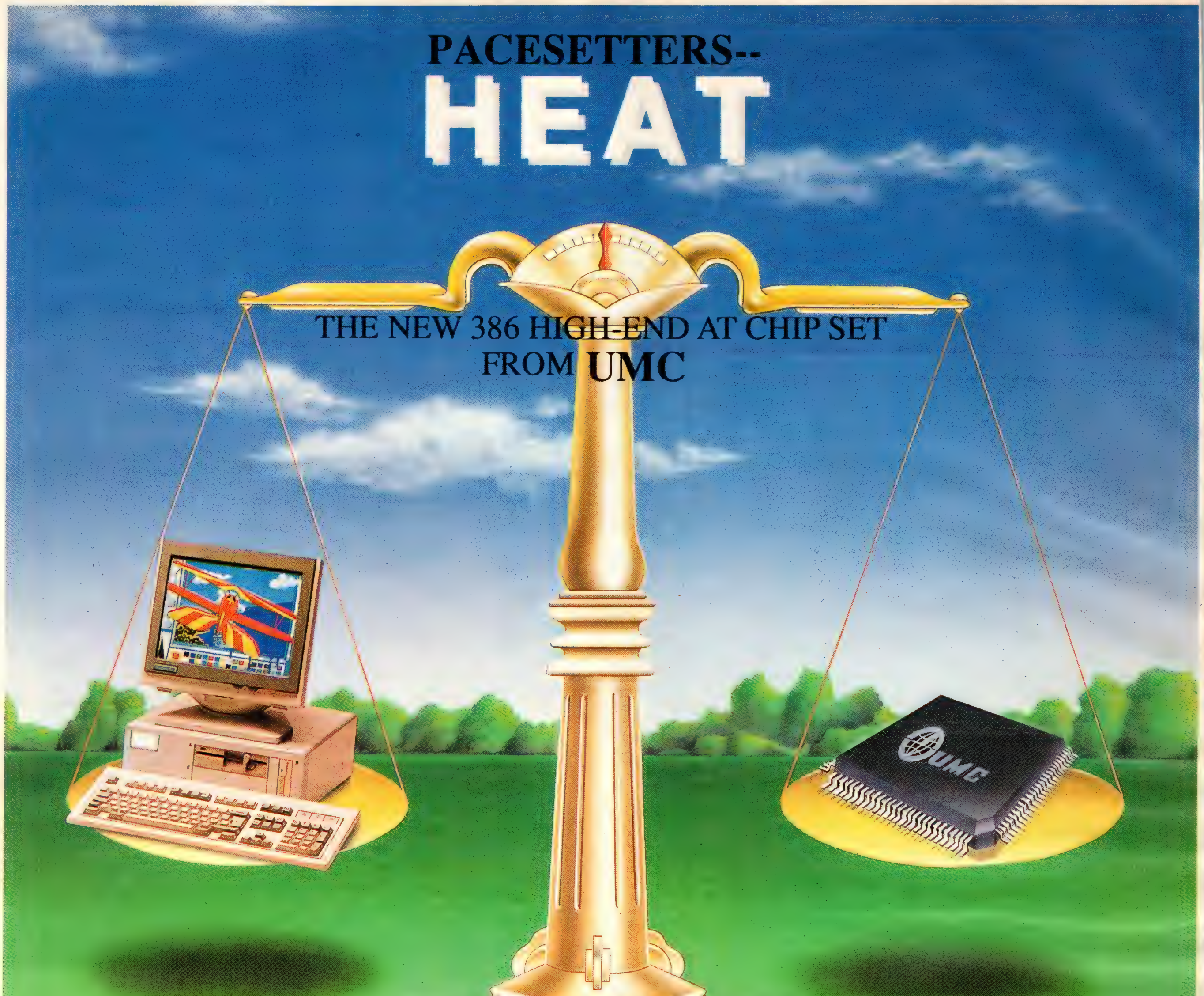

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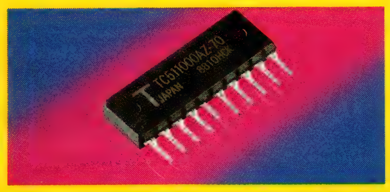

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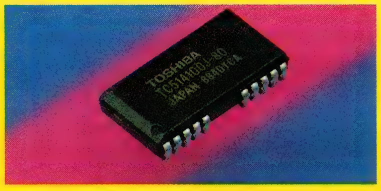

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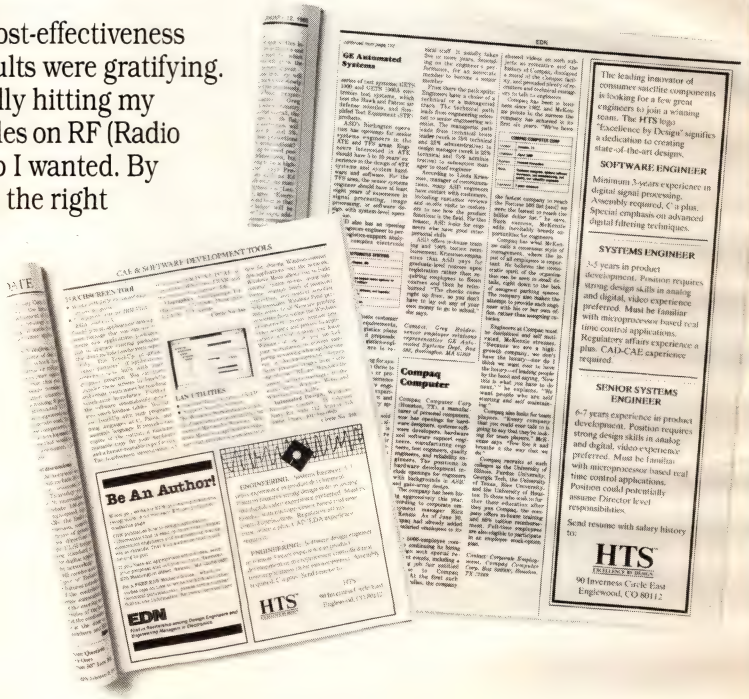

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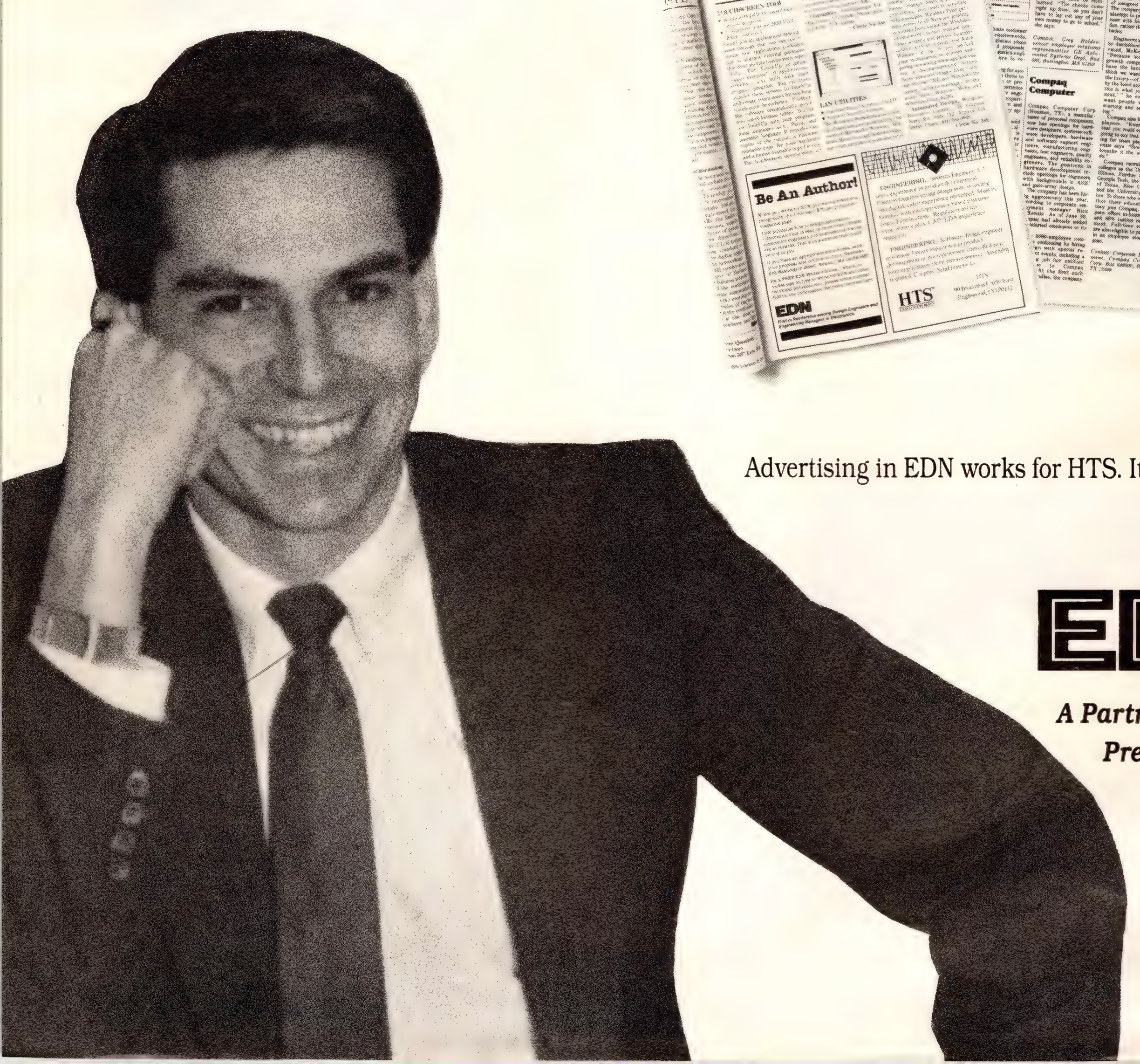

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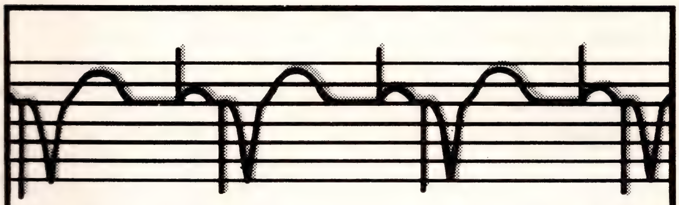

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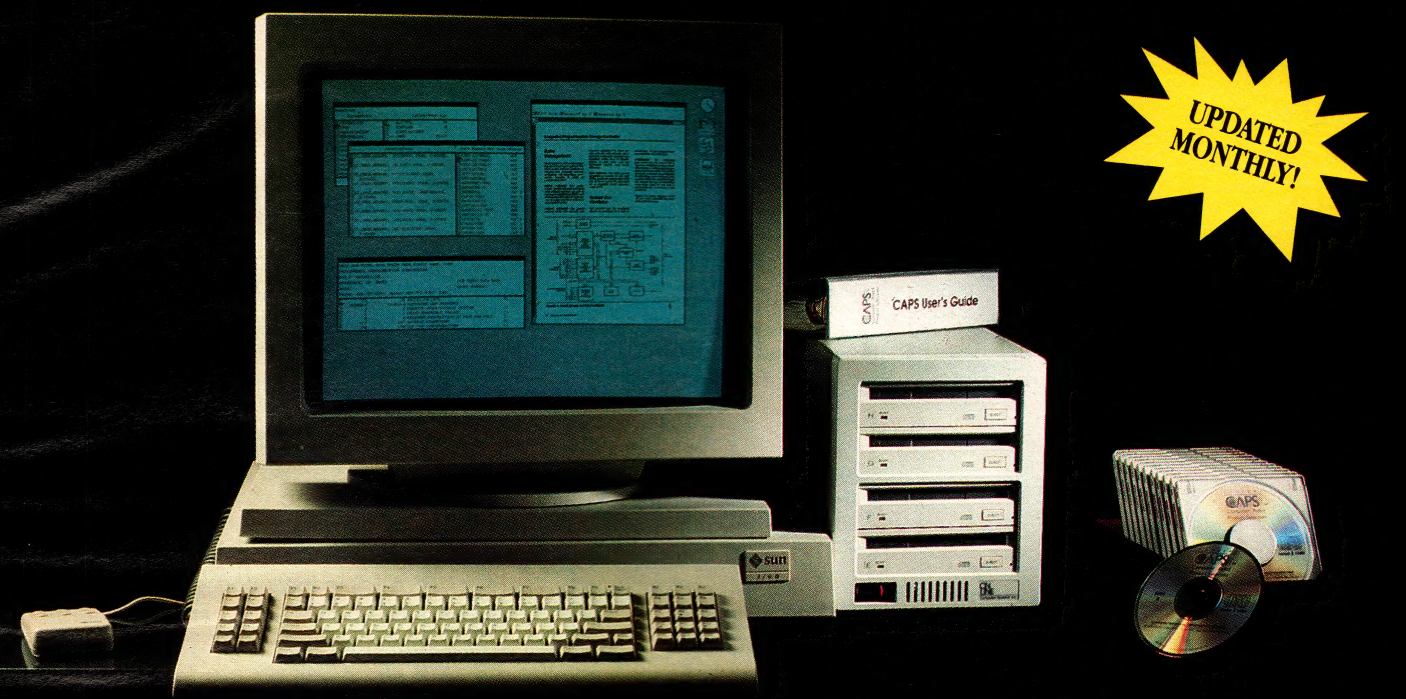

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Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95** **$69.95**		**$48.95** **$79.95**	

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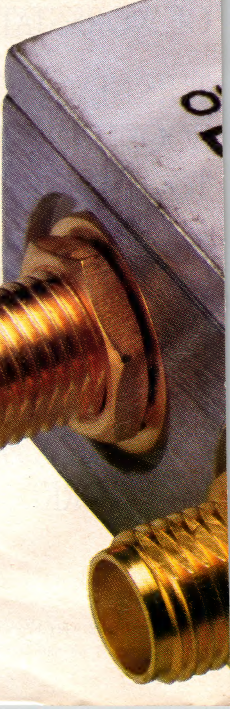

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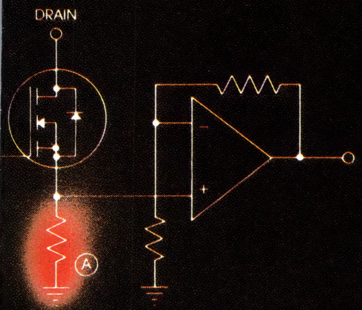
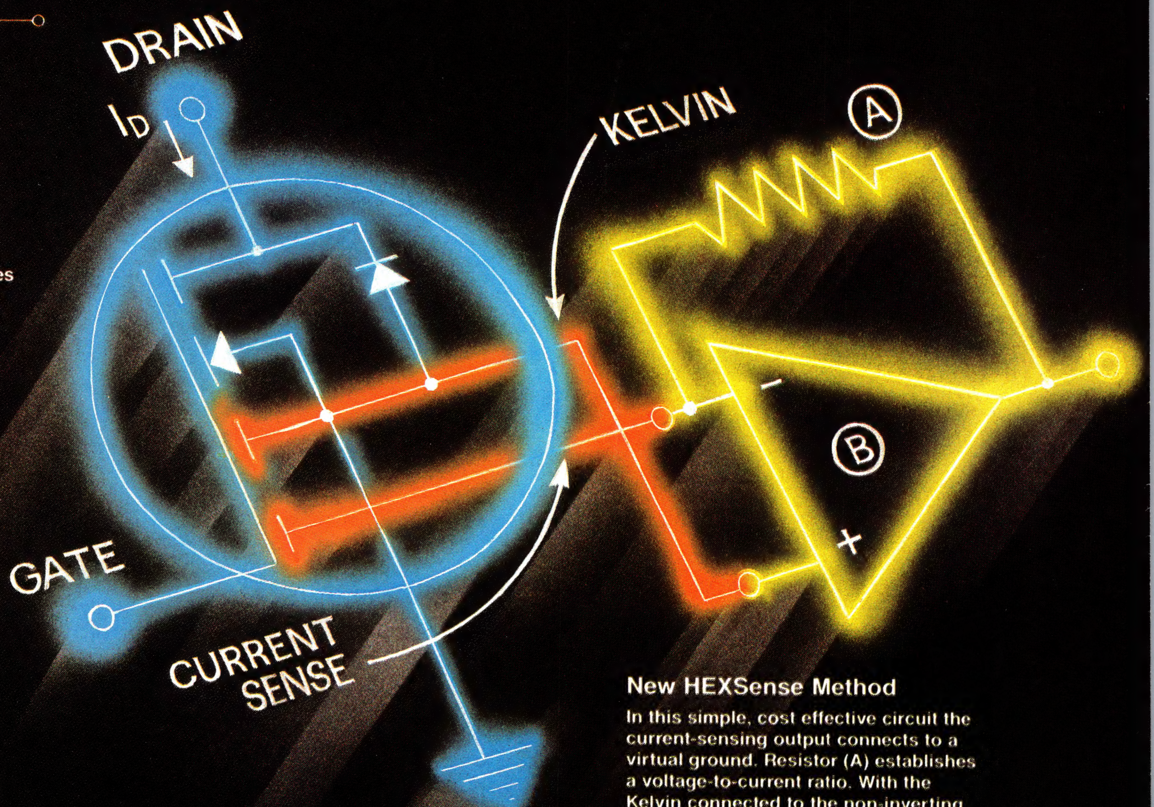


d Method

is circuit uses a fractional value istor (A) to measure current, using a voltage drop which increases wer losses. Its parasitic inductance o slows down switching speed. To set these losses, a lower $R_{DS(ON)}$ wer MOSFET may be used, reasing circuit cost.



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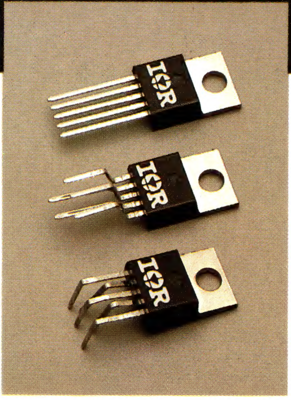

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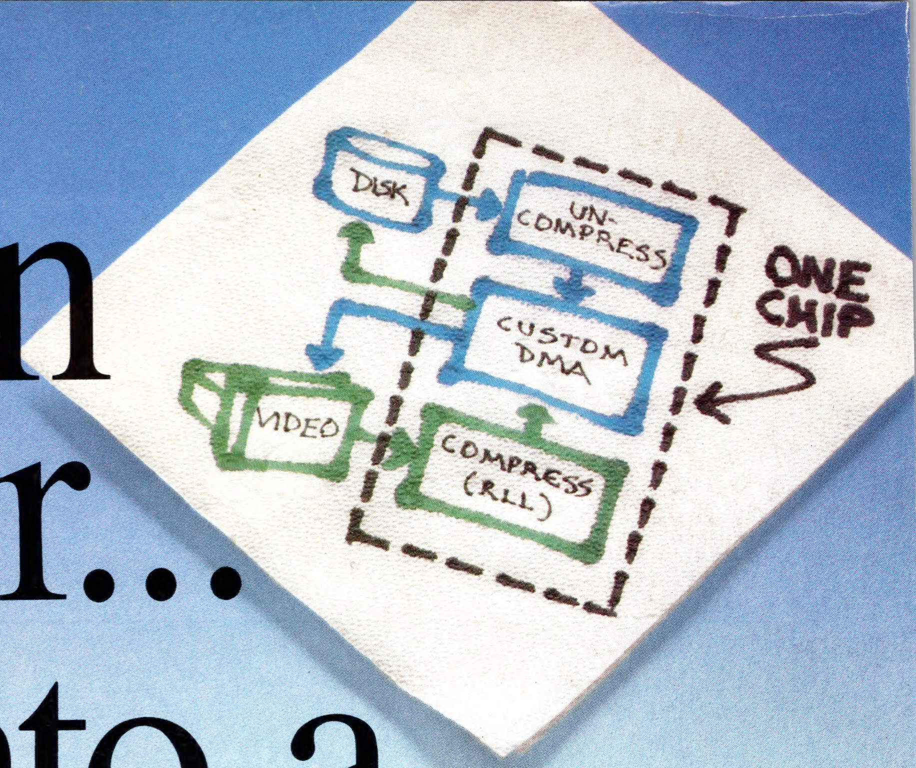

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